



AuthenTec, Inc.
Personal Security for the Real World™

EntréPad AES2501A FINGERPRINT SENSOR

Product Specification For Universal Serial Bus Applications



Hardware Reference

2317 Rev 1.1
November 17, 2004

AuthenTec Confidential Information



AuthenTec, Inc.
Post Office Box 2719
Melbourne, Florida 32902-2719
321-308-1300
www.authentec.com



AuthenTec welcomes your suggestions. We try to make our publications useful, interesting, and informative, and we hope you will take the time to help us improve them. Please send any comments or suggestions by mail or e-mail.

Disclaimer of Warranty

AUTHENTEC SOFTWARE, INCLUDING INSTRUCTIONS FOR ITS USE, IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY KIND. AUTHENTEC FURTHER DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR OF FITNESS FOR A PARTICULAR PURPOSE. THE ENTIRE RISK ARISING OUT OF THE USE OR PERFORMANCE OF THE SOFTWARE AND DOCUMENTATION REMAINS WITH YOU.

IN NO EVENT SHALL AUTHENTEC, ITS AUTHORS, OR ANYONE ELSE INVOLVED IN THE CREATION, PRODUCTION, OR DELIVERY OF THE SOFTWARE BE LIABLE FOR ANY DAMAGES WHATSOEVER (INCLUDING, WITHOUT LIMITATION, DAMAGE FOR LOSS OF BUSINESS PROFITS, BUSINESSINTERRUPTION, LOSS OF BUSINESS INFORMATION, OR OTHER PECUNIARY LOSS) ARISING OUT OF THE USE OF OR INABILITY TO USE THE SOFTWARE OR DOCUMENTATION, EVEN IF AUTHENTEC HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES. BECAUSE SOME STATES OR COUNTRIES DO NOT ALLOW THE EXCLUSION OR LIMITATION OF LIABILITY FOR CONSEQUENTIAL OR INCIDENTAL DAMAGES, THE ABOVE LIMITATION MAY NOT APPLY TO YOU.

U.S. Government Restricted Rights

AuthenTec software and documentation are provided with RESTRICTED RIGHTS. Use, duplication, or disclosure by the government is subject to restrictions as set forth in subparagraph (c)(1)(ii) of the Rights in Technical Data and Computer Software clause at DFARS 252.227-7013 or subparagraph (c)(1) and (2) of the Commercial Computer Software – Restricted Rights 48 CFR 52.227-19, as applicable. Manufacturer is AuthenTec, Inc.; Melbourne, Florida 32901-2719. This Agreement is governed by the laws of the State of Florida.

AuthenTec, Inc.
Post Office Box 2719
Melbourne, Florida 32902-2719
321-308-1300
www.authentec.com
apps@authentec.com

AuthenTec, FingerLoc, EntréPad, Aware, AES2501A, AES3550, AES4000, AF-S2, ISX, TruePrint, the AuthenTec colophons and logotypes, and the phrase "Personal Security for the Real World" are trademarks of AuthenTec, Inc. Microsoft and Windows 98 are registered trademarks of Microsoft Corp. Microwire™ is a trademark of National Semiconductor Corp. SPI™ is a registered trademark of Motorola. All other trademarks are the property of their respective owners.

Product Specification for the AES2501A Fingerprint Sensor

Copyright ©2004 by AuthenTec, Inc. No part of this publication may be reproduced in any form or by any means without prior written permission. Printed in the United States of America.

Table of Contents

1. INTRODUCING THE ENTRÉPAD AES2501A SLIDE SENSOR.....	6
1.1 TRUEPRINT TECHNOLOGY IS.....	6
1.2 FEATURE SUMMARY.....	6
1.3 CONVENTIONS.....	7
1.4 OPERATIONAL DESCRIPTION.....	7
1.5 NAVIGATION USING THE AES2501A.....	8
2. DC ELECTRICAL CHARACTERISTICS	9
2.1 ABSOLUTE MAXIMUM RATINGS	9
2.2 RECOMMENDED OPERATING CONDITIONS	9
2.3 DC CHARACTERISTICS @ RECOMMENDED OPERATING CONDITIONS.....	10
3. SENSOR OPERATION	11
3.1 OPERATION DESCRIPTION	11
3.2 INTERNAL CHIP BLOCK DIAGRAM	12
4. PACKAGING & PIN DEFINITIONS	13
4.1 PACKAGING INFORMATION.....	13
4.2 PIN LIST	15
4.2.1 <i>Pin Type and Activity Definitions</i>	16
4.3 PIN DESCRIPTIONS.....	17
4.4 CLOCK SELECT CONTROL	18
4.4.1 <i>Clock Specification</i>	18
4.5 TIMING INFORMATION	20
4.5.1 <i>Image Scan Timing</i>	20
4.5.2 <i>USB Interface</i>	20
4.5.3 <i>Finger Detect Auto-calibration</i>	20
5. SYSTEM INTERFACE DESCRIPTIONS	21
5.1 INTERFACE SELECT CONTROL	21
5.2 USB INTERFACE	22
5.3 RESET.....	24
6. SOFTWARE INTERFACE DETAILS	25
6.1 REGISTER MAP.....	25
6.1.1.1 Control Register 1 (CTRL1) (80h).....	27
6.1.1.2 Control Register 2 (CTRL2) (81h).....	28
6.1.1.3 Excitation Common Controls (EXCITCTRL) (82h).....	29
6.1.1.4 Detect Control (DETCTRL) (83h)	30
6.1.1.5 Navigation Correlation Range (NAVCORRNGE) (84h)	31
6.1.1.6 Navigation Finger Detect Threshold (NAVFDTHRS) (85h)	31
6.1.1.7 Navigation Control (NAVCTRL) (86h).....	32
6.1.1.8 Detect Frequency (DEFREQ) (87h).....	33
6.1.1.9 Column Scan Rate (COLSCAN) (88h).....	34
6.1.1.10 Measure Drive (VDCTRLMD) (89h).....	35
6.1.1.11 Measure Frequency (MEASFREQ) (8Ah).....	36
6.1.1.12 Demod Phase 1(DEMODPHASE1) (8Ch)	37
6.1.1.13 Channel Gain (CHANGAIN) (8Eh).....	38
6.1.1.14 Channel Bias (CHANBIAS) (8Fh)	39
6.1.1.15 Carrier Null (CARRNULL) (90h).....	40
6.1.1.16 A/D Reference High (ADREFHI) (91h)	41
6.1.1.17 A/D Reference Low (ADREFLO) (92h).....	41
6.1.1.18 Start Column (STRTCOL) (95h)	42
6.1.1.19 End Column(ENDCOL) (96h)	42



6.1.1.20	Data Format (DATFMT) (97h).....	43
6.1.1.21	Image Data Control (IMAGCTRL) (98h)	44
6.1.1.22	GPIO Data (GPIODATA) (99h).....	45
6.1.1.23	Sensor Status (STAT) (9Ah).....	46
6.1.1.24	Challenge Word 1 (CHWORD1) (9Bh)	47
6.1.1.25	Challenge Word 2 (CHWORD2) (9Ch)	47
6.1.1.26	Challenge Word 3 (CHWORD3) (9Dh).....	48
6.1.1.27	Challenge Word 4 (CHWORD4) (9Eh).....	48
6.1.1.28	Challenge Word 5 (CHWORD5) (9Fh).....	48
6.1.1.29	Test Register 1 (TREG1) (A1h)	49
6.1.1.30	FD Threshold (FDTHRESHOLD) (A8h).....	50
6.1.1.31	Miscellaneous Control (MISCCTRL) (ACh)	51
6.1.1.32	Single Reg. Address (SREGADDR) (ADh).....	52
6.1.1.33	FDRV X HI (FDRVXHI) (AEh).....	53
6.1.1.34	FDRV X LO (FDRVXLO) (AFh).....	53
6.1.1.35	Watchdog Control (WDCtrl) (B0h)	54
6.1.1.36	Misc. Image Control/GPIO Disable(MISCCTRL) (B3h).....	55
6.1.1.37	SOF Timestamp/FreeRun[13:7] (SOFTIMEHIGH) (BAh)	56
6.1.1.38	SOF Timestamp/FreeRun[6:0] (SOFTIMELOW) (BBh)	56
6.1.1.39	EOF Timestamp[13:7] (EOFTIMEHIGH) (BCh).....	56
6.1.1.40	EOF Timestamp[6:0] (EOFTIMELOW) (BDh).....	57
7.	DATA FORMATS	58
7.1	OVERVIEW	58
7.1.1	Registers Message Format	59
7.1.2	Image Data Format – Grey Scale 500 ppi.....	59
7.1.3	Image Data Format – 250 ppi.....	60
7.1.4	Image Data Format – Monochrome	61
7.1.5	Histogram Message Format	62
7.1.6	Authentication Word Message Format.....	63
8.	PART NUMBERING SCHEME.....	64
9.	REVISION HISTORY	65



LIST OF FIGURES

Figure 1-1	Row Numbering.....	7
Figure 2-1	Absolute Maximum Ratings.....	9
Figure 2-2	Recommended Operating Conditions	9
Figure 2-3	DC Characteristics.....	10
Figure 3-1	AES2501A Functional Diagram.....	11
Figure 3-2	Internal Chip Block Diagram.....	12
Figure 4-1	Pin List by Interface	16
Figure 4-2	AES2501A Active Pin Functional Description	17
Figure 4-3	External Clock Specifications	19
Figure 5-2	SIO Pin Definitions for the USB Interface.....	21

LIST OF TABLES

Table 4-1	CLKSEL[2:0] Decode	18
Table 5-2	Device Descriptor	22
Table 5-3	Default Configuration Descriptor	23
Table 5-4	Default Interface 0, Alternate Setting 0 Descriptor	23
Table 5-5	Default Interface 0, Alternate Setting 0, Bulk Endpoint Descriptors	23
Table 5-6	String 0 Descriptor	24
Table 6-1	Registers Summary	26
Table 7-1	Command Byte Definition	58
Table 7-2	Gray Scale Message Format	59
Table 7-3	4 Bit 250 ppi Gray Scale Message Format	60
Table 7-4	Monochrome Packed Message Format	61
Table 7-5	Histogram Message Format	62
Table 7-6	Authentication Word Message Format	63

1. Introducing the EntréPad AES2501A Slide Sensor...

..., the latest, lowest cost fingerprint sensor IC for PC Applications. AuthenTec has adapted its patented, award winning TruePrint Technology to read fingerprints while the finger is pulled across the AES2501A's rectangular surface. In this manner, the fingerprint images are acquired AND the sensor is substantially reduced in size.

The AES2501A combines silicon-based image slice capture with proprietary sensor control and image segment matching algorithms to provide the best quality lowest cost biometric authentication solution available.

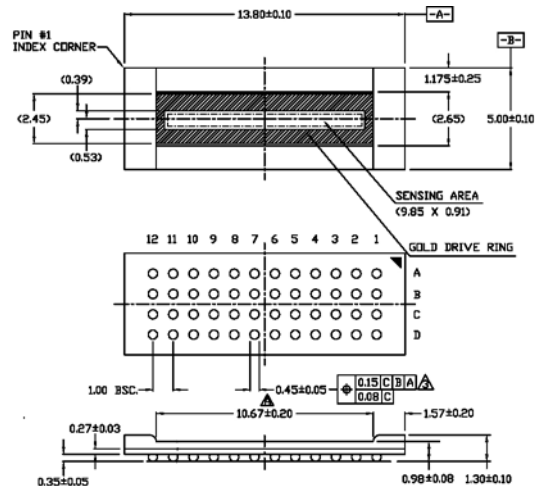
1.1 TruePrint Technology is...

...AuthenTec's unique patented fingerprint reading technology. During imaging, a small signal is generated between the IC and the finger's living tissue layer. 3072 individual sensing elements in the slide sensor matrix form a planar antenna array that receives this signal, creating a digital pattern that accurately reproduces the fingerprint's underlying structure.

A powerful utility contained within TruePrint Technology™ is Dynamic Optimization™. This tool analyzes each image, controlling up to 15 parameters real-time to optimize the fingerprint image slices, regardless of unusual skin conditions or surface contamination. This functionality is built right into the sensor hardware or you can perform these functions in software for total control and upgrade-ability.

1.2 Feature Summary

- ✓ Patented TruePrint Technology for best Ability To Acquire (ATA)
- ✓ High Definition 192 X 16 TruePrint Technology Based Pixel Array
 - 500 pixels per inch (ppi) native
 - 9.75mm X 0.81mm array area
- ✓ Compact 48 Ball Grid Array (BGA) Package
 - 13.8mm X 5mm X 1.3mm
- ✓ USB Operating Voltage Range
 - 3.0V to 3.6V single supply
- ✓ 0°C to +70°C operating temperature range
- ✓ Easy to Integrate USB 2.0 Full Speed
- ✓ Operation with Crystal, Resonator, or with external clock input
- ✓ Ultra-hard scratch resistance surface coating
 - > 1 Million rubs w/o degradation
- ✓ IEC 61000-4-2 Level 4 ESD Capability (+/- 15KV)
- ✓ Built-in low power Finger Detection w/system interrupt capability
- ✓ Multiple battery-friendly operating modes @ 3.3V
 - Imaging @ <40mA typ.
 - 5-way Navigation @ < 3mA typ.



1.3 Conventions

For vectors (groups of bits), ordering will always be from MSB to LSB (e.g. Pixel_Data[63:0] where bit 63 is the MSB and bit 0 is the LSB).

When vectors that span multiple bytes are transmitted, the lower byte (bits [7:0]) is transmitted first. This applies to pixel data and the authentication word returned after each imaging frame.

Numbers followed by a 'b' are shown in binary. Numbers followed by an 'h' are in hexadecimal.

1.4 Operational Description

The Sensor begins operation in the 'idle' state after a reset. In the idle state, array power is turned off and clocking is disabled (except to support interface activity). It is then necessary for the system SW to program the sensor for the desired operation (Imaging or Navigation). After this setup, the requested operation is enabled by setting the Op Enable bit (located in Register 80h:D2). If Imaging is selected, the Sensor enters finger detect mode checks for a finger present at a rate programmed by the Finger Detect Rate setting. The default reset value sets the detect period to ~62 ms.

After finger detection, the sensor will begin the programmed operation and will enter Imaging mode until the finger is removed. Once the finger is removed, the sensor returns to the Low Power Finger Detect mode. When no activity is detected on the system interface bus for approximately 200uS, power is reduced by disabling the internal clocks and the array power is once again turned off.

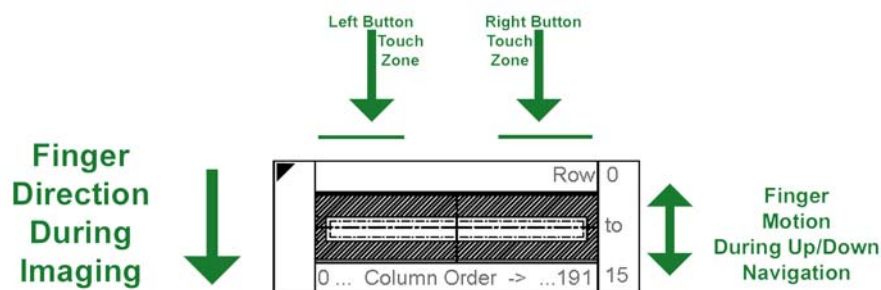


Figure 1-1 Row Numbering

The array consists of 192 columns of 16 pixels each. During imaging, the columns are powered up and the signals from each of the 16 pixels/column are sampled, digitized and returned to the host computer over the selected interface sequentially in order on a per-column basis. The sensor has the capability to utilize only the center 128 columns during imaging mode to facilitate higher finger sliding speeds. During fingerprint enrollment, a 192 pixel wide template is created. Then, optionally, either a 192 pixel wide or 128 pixel wide verify can be performed. This mode is entirely controlled via software using sensor register settings for start and stop columns.

If the finger detect is not active when it is rechecked at the end of a scan, the array is powered down and the sensor reverts back to checking for a finger at the programmed detect rate.

AuthenTec has application notes to support the integration of the AES2501A for all available interface options. Contact AuthenTec for availability.

1.5 Navigation Using the AES2501A

The navigation use model is a button replacement system. The typical Left / Right / Up / Down button functionality can be easily emulated on the sensor by statically touching the sensor to indicate desired left or right direction and by sliding the finger at normal finger speeds in the up or down direction to indicate up or down.

When operations are enabled (via the OP ENABLE bit as described previously) and Navigation mode is selected, the sensor will provide constant, periodic indications of direction and finger presence by sending a 2-byte message to the selected interface.

After NAV mode is enabled, the sensor takes 10 samples of the center column approximately every 100 us. After producing an output message, the sensor then enters a low power state for a programmable amount of time, and then repeats the above sequence. Output generation rates are programmable and range from 100 Hz down to 26 Hz.

2. DC ELECTRICAL CHARACTERISTICS

2.1 Absolute Maximum Ratings

An absolute maximum rating is the maximum value guaranteed by the AuthenTec. The use of a product in violation of these ratings can result in significant loss of device reliability or cause damage to the IC.

Symbol	Parameter	Min.	Max.	Units
V_{DD}	Supply Voltage	-0.5	4.3	V
V_I	Input Voltage	-0.5	$V_{DD}+0.5$	V
V_O	Output Voltage	-0.5	$V_{DD}+0.5$	V
I_{IK}	Input Clamp Current $V_I < V_{SS}$ or $V_I > V_{DD}$		± 20	mA
I_{OK}	Output Clamp Current $V_O < V_{SS}$ or $V_O > V_{DD}$		± 20	mA
T_{STG}	Storage Temperature	-65	150	°C
Latch-Up	Latch-Up Immunity JEDEC JESD78	± 100		mA
T_{SOL}	Soldering Temperature		+240	°C
ESD_{PIN}	Pin-level ESD Immunity JESD22 Method A114-B	-2000	+2000	V
$ESD_{PACKAGE}$	Package-level ESD Immunity IEC61000-4-2 Level 4 Air Discharge method using AuthenTec approved reference design	-15	+15	KV

Figure 2-1 Absolute Maximum Ratings

2.2 Recommended Operating Conditions

Symbol	Parameter	Min.	Typ	Max.	Units
V_{DD}	Supply Voltage	3.0	3.3	3.6	V
$V_{DDACp-p}$	Power Supply Ripple	-50	0	+50	mV
V_I	Input Voltage	0		V_{DD}	V
V_O	Output Voltage	0		V_{DD}	V
V_{IH}	High Level Input Voltage	$70\% V_{DD}$		V_{DD}	V
V_{IL}	Low Level Input Voltage	0		$30\% V_{DD}$	V
t_t	Input Transition (Rise and Fall) Time	0		3	ns
T_A	Ambient operating temperature	0		70*	°C

Figure 2-2 Recommended Operating Conditions

***Warning**

The AES2501A remains fully operational at temperatures that are high enough to be uncomfortable for the user.

For reasons of safety and protection, AuthenTec reference designs include circuitry that serves to manage the junction temperature by controlling the supply current. If the hardware developer elects not to use the AuthenTec-provided control circuit design, it will then be essential that an equivalent design be developed and implemented.

2.3 DC Characteristics @ Recommended Operating Conditions

Unless otherwise specified, $V_I = V_{DD}$ or V_{SS} , $T_{Ambient} = 25^{\circ}C$

Symbol	Parameter	Conditions	Min.	Typ	Max.	Units
V_{OH}	High Level Output Voltage	$I_{OH}=2mA$	$V_{dd}-0.3$			V
V_{OL}	Low Level Output Voltage	$I_{OL}=2mA$			0.3	V
I_{IL}	Low Level Input Current	$V_I=V_{IL}(min.)$			± 1	μA
I_{IH}	High Level Input Current	$V_I=V_{IH}(max.)$			± 1	μA
I_{OZ}	High Impedance State Output Current				± 20	μA
USB Interface Supply Currents						
I_{DDQ}	Supply Current Imaging mode; USB (peak)	$V_{dd}=3.3V$		45		mA
I_{DDQ}	Supply Current Navigation or Finger Detect; USB	$V_{dd}=3.3V$		3		mA
I_{DDQ}	Supply Current Suspend Current; USB	$V_{dd}=3.3V$		350		μA

Figure 2-3 DC Characteristics

All I_{DDQ} Currents measured RMS using standard AuthenTec software and drivers. Use of other software or customized register settings may effect actual power consumption.

3. SENSOR OPERATION

3.1 Operation Description

During an imaging event, the RF TruePrint Signal is conducted via the Drive Ring to the users' finger. The TruePrint Signal is then conducted through and modulated by the "live layer" of the finger where the true fingerprint originates. The imaging array (center strip region of the chip) measures the TruePrint signal; the strength of which corresponds to either a ridge or valley region.

The image array of the AES2501A sensor is composed of 16x192 pixels. The array is scanned similarly to a sub-array in AuthenTec's touch sensors. During the imaging process, 16 pixels in a column are powered up, sampled, and converted to 4-bit or 2-bit values. The high and low reference voltages for the ADC are programmable via 7-bit DACs.

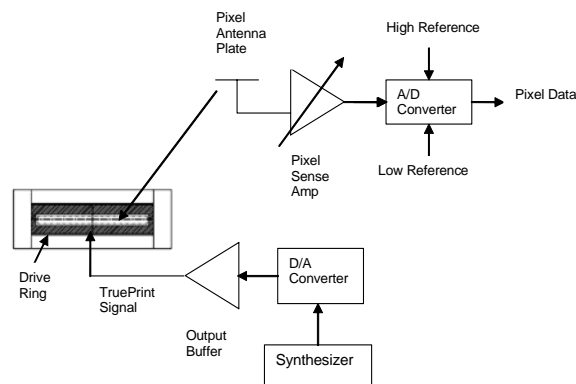


Figure 3-1 AES2501A Functional Diagram

The sensing element of each pixel is an RF sense-amplifier, which picks up the TruePrint (high frequency AC) signal (125 KHz – 2MHz) that is applied to the finger via the Finger Drive Ring, located prominently on the sensor surface which fully encloses the pixel array. The pixel sense amps receive, amplify, and buffer the signal.

Each pixel output is then converted into a level corresponding to the strength of the received signal. Stronger signals are picked up from ridges than valleys. This output is converted by an A/D converter whose endpoints are adjustable via the Reference High and Reference Low voltages.

3.2 Internal Chip Block Diagram

The following diagram shows a top-level block diagram of the Sensor IC.

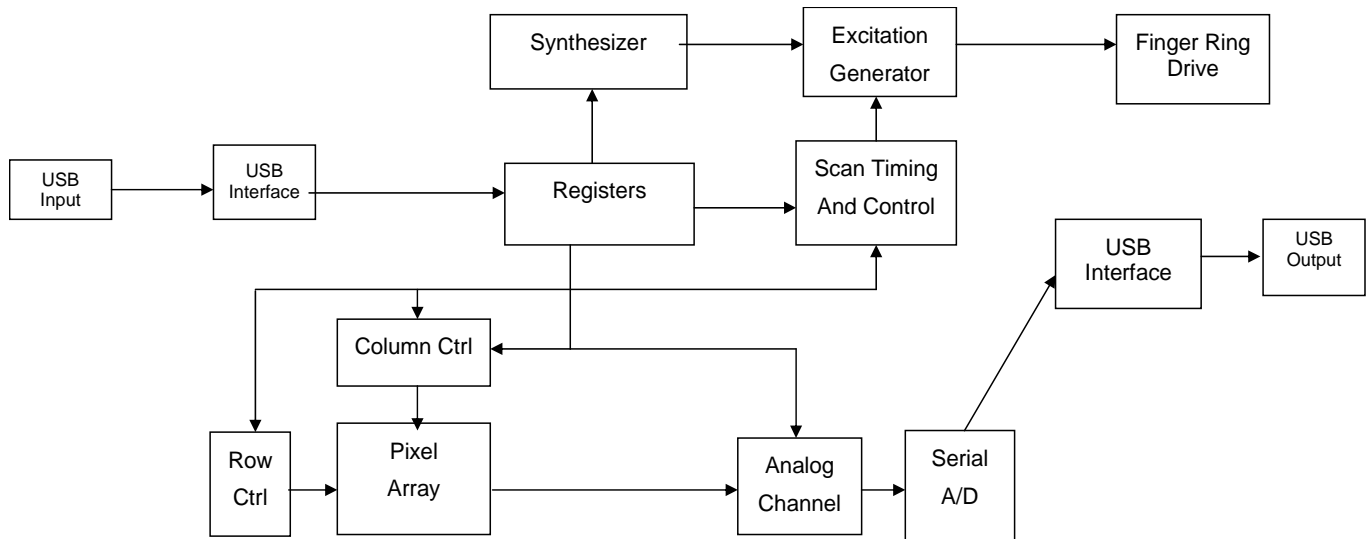


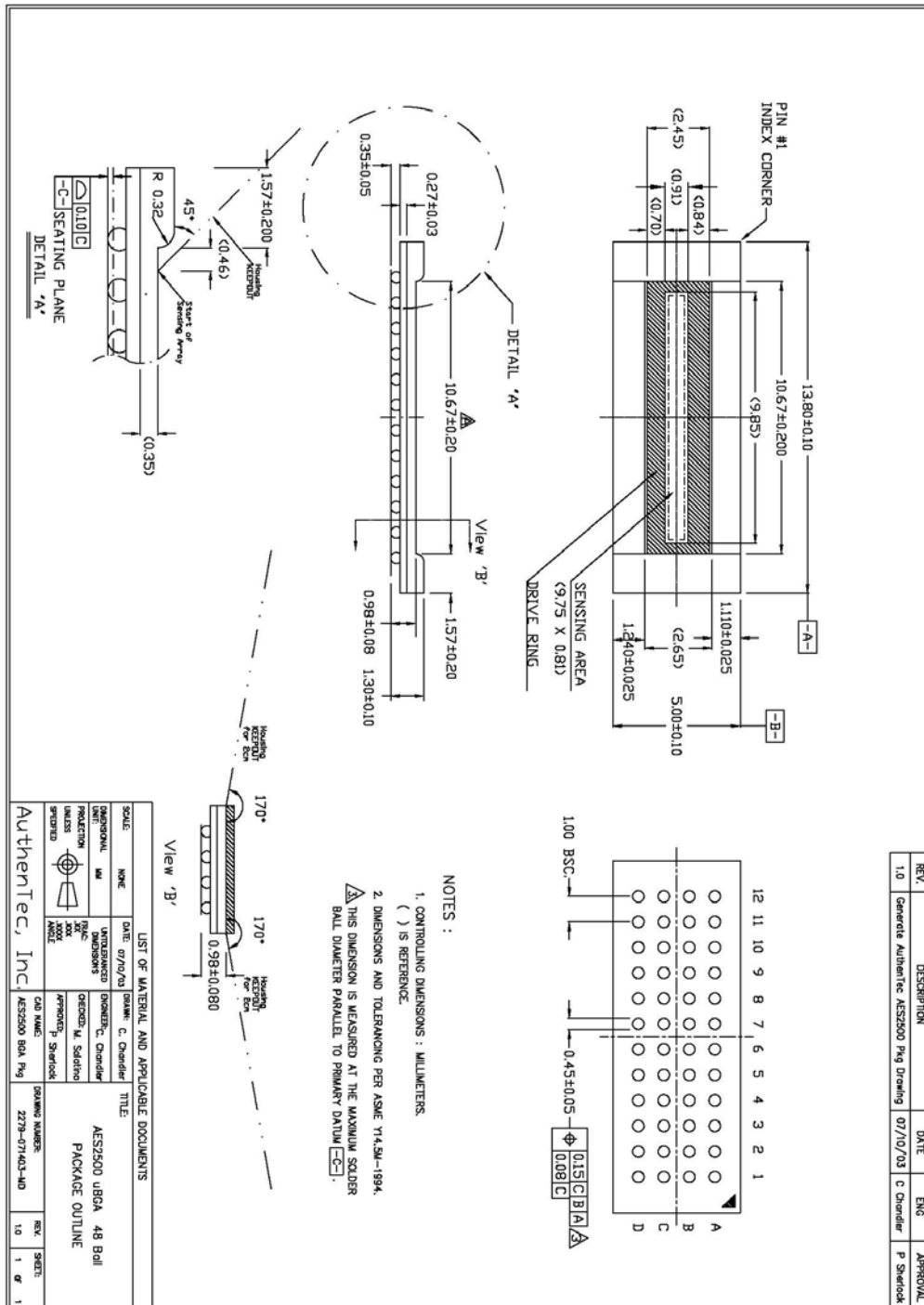
Figure 3-2 Internal Chip Block Diagram

4. Packaging & Pin Definitions

4.1 Packaging Information

The AES2501A sensor is housed in a plastic 48 Ball Grid Array package. The most current PDF version of this package drawing can always be viewed, printed, or downloaded at:

http://www.authentec.com/products/docs/AES2501A_48_BGA_Pkg.pdf



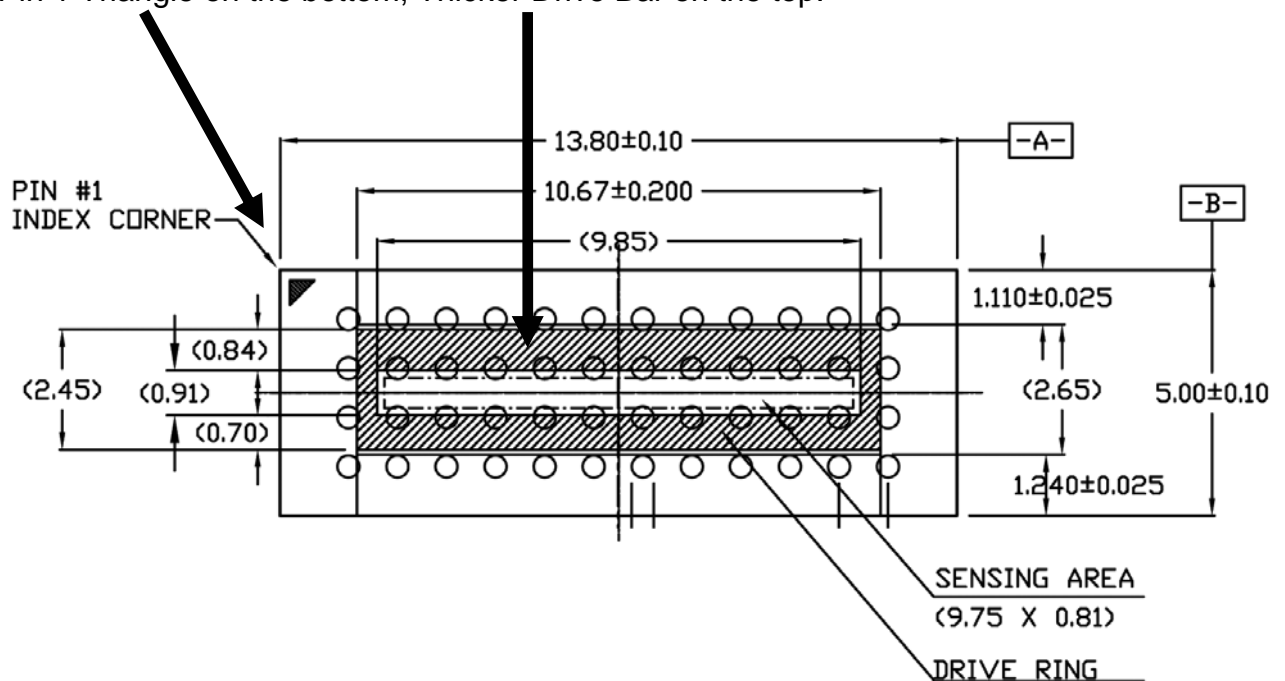
The package drawing shows both the mechanical dimensions of the package as well as recommended housing “keep-out” areas and angles of approach to and from the slide surface. For additional information, contact AuthenTec Applications Engineering for more details.

The Pin 1 indicator is a gold triangle located in the corner of the package adjacent to pin one.

Post-assembly top-side inspection can be performed visually using the fact that the drive bars are of different thickness (One Bar is 0.84mm, the other is 0.70mm). When the thicker drive bar is located at the top of the device from the inspection viewpoint, pin one is located top left from the same perspective.

The “X-Ray” view below shows the perspective described.

Pin 1 Triangle on the bottom, Thicker Drive Bar on the top.



4.2 Pin List

Pin assignments and pin function descriptions of the AES2501A sensor are given below. Shared pin definitions for SIO[8:0] are selected by the state of the IOSEL[1:0] pins. Refer to section 5.1 for the interface-specific SIO definitions. The following pin lists match AuthenTec certified reference designs. Certain pin functions will be required to change for other implementations.

Pin	Type	Digital Activity	Signal Name (USB)
A1	Passive	Static	VREF
A2	Passive	Static	CT2
A3	Passive	Static	CT1
A4	Output	Active	FINGERDRIVE
A5	Input	Static	RESET*
A6	Reserved		N/C
A7	Reserved		N/C
A8	Power		VDD
A9	Power		GND
A10	Passive	Static	PLL_FILTER
A11	Input	Active	SYS_CLK
A12	Output	Active	DRIVE_RING
B1	Input	Static	CLKSEL2
B2	Power		GND
B3	Power		VDD
B4	Input	Static	VDDL
B5	Input	Static	VDDL
B6	Input	Static	CLKSEL1
B7	I/O	Active	SUSPEND
B8	I/O	Active	USB_OE*
B9	I/O	Active	D+
B10	I/O	Active	D-
B11	I/O	Active	PID3
B12	I/O	Active	PID2
C1	Reserved		N/C
C2	Power		VSS
C3	Power		VDDA
C4	Input	Static	VSSL
C5	Input	Static	CLKSEL0
C6	Input	Static	VSSL
C7	I/O	Active	PID0
C8	I/O	Active	PID1
C9	I/O	Active	ENUM
C10	Output	Active	VDDA_ON*
C11	Power		VSS
C12	Power		VDDA
D1	Output	Active	DRIVE_RING
D2	Reserved		N/C
D3	Reserved		N/C
D4	Reserved		N/C

Pin	Type	Digital Activity	Signal Name (USB)
D5	Reserved		N/C
D6	Reserved		N/C
D7	Reserved		N/C
D8	Power		OVC_VDD
D9	Output	Static	OVC_DET
D10	Power		OVC_VDDA
D11	Input	Static	OVC_SENSE
D12	Power		VSS

Figure 4-1 Pin List by Interface

4.2.1 Pin Type and Activity Definitions

Power:	Power Supply Connections
Passive:	Connections to passive components (ex: Filter caps, etc)
Input:	Active Inputs to the sensor
Output:	Active Outputs from the sensor
I/O:	Active I/O's from the sensor (state / configuration dependent)
Reserved:	Do Not Connect anything to these pins
Static:	DC or slowly changing voltages
Active:	Active Signals, Digital or Analog
VDDL:	Fixed Active High Logic Level
VSSL:	Fixed Active Low Logic Level
VDDA:	Pixel Array Power supply pin

4.3 Pin Descriptions

Pin	Signal Name	Function Description
		For pins D8-D12, Refer to the appropriate AuthenTec Reference Design for connection details
C5	CLKSEL0	Clock input option selection. Refer to section 4.4
B6	CLKSEL1	Clock input option selection. Refer to section 4.4
B1	CLKSEL2	Clock input option selection. Refer to section 4.4
A3	CT1	Filter Capacitor - connect to pin A2 through a 0.1uF capacitor, standard bypass type
A2	CT2	Filter Capacitor - connect to pin A3 through a 0.1uF capacitor, standard bypass type
D1	DRIVERING	DriveRing - connection to the metal ring on the sensor surface. No other connections made.
A12	DRIVERING	DriveRing - connection to the metal ring on the sensor surface. No other connections made.
A4	FINGERDRIVE	TruePrint Signal output used to drive radio frequency signal through external circuitry to finger ring pins (A12 and D1). Controlled by internal excitation generator.
D9	OVC_DET	Over Current Detect Power Off output - Active low for power on. Refer to reference design schematics for connection details.
D11	OVC_SENSE	Load side of current sense resistor input for over current control. Refer to Ref. Design
D8	OVC_VDD	Over Current Detect Circuit Digital Power Supply Pin (V) Refer to Ref. Design
D10	OVC_VDDA	Over Current Detect Circuit Analog Power Supply Pin (V) Refer to Ref. Design
A5	RESET*	Reset input - 2/3 threshold voltage with hysteretic input. Approximately 57 Kohm pull-up resistor internal, with tolerance of 30%. See section 5.3 for additional definition of a proper reset.
B8	SIO0	Refer to Figure 5.1
B7	SIO1	Refer to Figure 5.1
C7	SIO2	Refer to Figure 5.1
C8	SIO3	Refer to Figure 5.1
B12	SIO4	Refer to Figure 5.1
B11	SIO5	Refer to Figure 5.1
B10	SIO6	Refer to Figure 5.1
B9	SIO7	Refer to Figure 5.1
C9	SIO8	Refer to Figure 5.1
A11	SYS_CLK	Clock input pin - input clock used for all chip functions. See Figure 4-3 and Section 4.4 for input characteristics and requirements.
C12	VDDA	Pixel Array Power Connection
C3	VDDA	Pixel Array Power Connection
C10	VDDA_ON*	External Array Power FET control - If used this pin may drive a high side P-channel FET. See AuthenTec Reference Designs for connection details.
A1	VREF	Voltage Reference output - to be connected to a capacitance of 0.22uF to ground, standard bypass type
D12	VSSOD	Over Current Detect Circuit Return Supply pin (GND)
A10	PLL_FILTER	Refer to USB Reference Design Schematic for appropriate filter components / connection

Figure 4-2 AES2501A Active Pin Functional Description



4.4 Clock Select Control

AES2501A can support a variety of clock sources, ranging in frequency from 6MHz up through 48MHz. The AES2501A uses a single pin crystal/resonator oscillator circuit that can also be overdriven with an external clock source. Clock frequency selection [including clocks driven into the SYS_CLK pin] is done via the CLKSEL[2:0] input pins. The following table shows the CLKSEL[2:0] pin configurations:

CLKSEL2 Pin B1	CLKSEL1 Pin B6	CLKSEL0 Pin C5	Crystal/Resonator or Clock Frequency
0	0	0	6 MHz
0	0	1	Reserved
0	1	0	12 MHz
0	1	1	18 MHz
1	0	0	24 MHz
1	0	1	Reserved
1	1	0	Reserved
1	1	1	48 MHz (PLL Bypass, clock only)

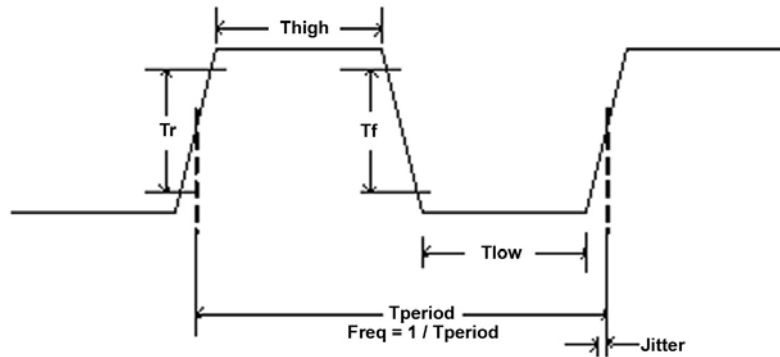
Table 4-1 CLKSEL[2:0] Decode

For USB applications, Crystal/Resonator frequency options include 6, 12, 18, and 24MHz.

4.4.1 Clock Specification

For the AES2501A, there are several different clocking options available: Crystal connection, ceramic resonator connection, and external clock driven. Appropriate application of clock sources is driven the desired circuit application (interface type) and reference design. This section addresses the specification requirements for an externally driven clock. All electrical and environmental conditions from the device specification apply as well.

When driving an external clock into the SYSCLK device pin, the following timing diagram applies:



[1] Parameter	[1] Minimum	[1] Maximum
[2] Freq. (USB Interface)	[2] 12MHz – 0.25%	[2] 12MHz + 0.25%
[3] Jitter (USB Interface)	[3]	[3] 0.2ns
[4] Tr	[4] -	[4] 3ns
[5] Tf	[5] -	[5] 3ns
[6] Thigh	[6] 45%*[Tperiod]	[6] 55%*[Tperiod]
[7] Tlow	[7] 45%*[Tperiod]	[7] 55%*[Tperiod]

Figure 4-3 External Clock Specifications

4.5 Timing Information

4.5.1 Image Scan Timing

The fastest scan time available is 32us per sixteen pixels and will limit image frame rates to less than $[16 \times 192 \text{ pixels} * 32 \text{us} / 16 \text{ pixels} = 6.144 \text{ ms}]$ or ~162.7 fps maximum. Transferring register data, histogram data, and authentication data will reduce this frame rate.

4.5.2 USB Interface

The AES2501A fingerprint sensor is as a USB low power device. This requires that the total current consumption be less than 100 mA and suspend current be less than 500uA. For all timing diagrams, please refer to the Universal Serial Bus Specification, Version 2.0. The AES2501A fully supports the USB selective suspend mode (C3 power state).

4.5.3 Finger Detect Auto-calibration

When using Finger Detect [delay method], the device is automatically calibrated once on power up. Sending a master reset to the device does not affect the setting of the reference delay value used for the finger detect calculation. If desired, the device can be re-calibrated by setting the Recalibrate FD bit [Reg82-D2], which is self-clearing.

5. System Interface Descriptions

5.1 Interface Select Control

For the USB interface, the following pin assignments apply:

SIO / Pin	USB (See section)	DIR
SIO0 / B8	USB_OE*	O
SIO1 / B7	SUSPEND	O
SIO2 / C7	PID0	I/O
SIO3 / C8	PID1	I/O
SIO4 / B12	PID2	I/O
SIO5 / B11	PID3	I/O
SIO6 / B10	D-	I/O
SIO7 / B9	D+	I/O
SIO8 / C9	ENUM	O

Figure 5-1 SIO Pin Definitions for the USB Interface

AuthenTec Vendor ID = 08FFh, Product ID= 258xh

5.2 USB Interface

The USB interface is compliant with version 2.0 of the USB specification for full speed interfaces. The AES2501A sensor is designed as a USB low power device.

The on-chip USB implementation utilizes 3 endpoints in one interface (endpoint 0, 1, and 2).

Endpoint 0 supports control read and write transactions, including String Descriptor support for the device identification function in Windows.

Endpoint 1 is a BULKIN endpoint for data going from the Sensor to the Host.

Endpoint 2 is a BULKOUT endpoint for Sensor commands from the Host.

The following Descriptor Tables are included to show the enumeration information for all USB configurations.

Field	Index	Value	Meaning
bLength	0	12h	Length of this descriptor = 18 bytes
bDescriptorType	1	01h	Descriptor Type = Device
bcdUSB(L)	2	10	USB spec. version 1.10 (L)
bcdUSB(H)	3	01	USB spec. version 1.10 (H)
bDeviceClass	4	FFh	Device class (FF is vendor specific)
bDeviceSubClass	5	FFh	Device sub-class (FF is vendor specific)
bDeviceProtocol	6	FFh	Device Protocol (FF is vendor specific)
bMaxPacketSize0	7	08h	Max Packet size for EP0 = 8 bytes
idVendor(L)	8	FFh	Vendor ID (L)
idVendor(H)	9	08h	Vendor ID (H)
idProduct(L)	10	8Xh	Product ID low byte programmed via PID[3:0]
idProduct(H)	11	25h	Product ID high byte
bcdDevice(L)	12	Device ID	Device ID (L)
bcdDevice(H)	13	Device ID	Device ID (H)
iManufacturer	14	00h	None
iProduct	15	01h	Product String – “Fingerprint Sensor”
iSerialNumber	16	00h	None
bNumConfigurations	17	01h	One configuration in this interface

Table 5-1 Device Descriptor

Field	Index	Value	Meaning
bLength	0	09h	Length of this descriptor = 9 bytes
bDescriptorType	1	02h	Type = Configuration
wTotalLength(L)	2	20h	Total Length(L) including Interface and Endpoint descriptors
wTotalLength(H)	3	00h	
bNumInterfaces	4	01h	Number of interfaces in this configuration
bConfigurationValue	5	01h	Configuration value used by Set_Configuration to select this interface
iConfiguration	6	00h	00h = no string reference
bmAttributes	7	A0h	A0h, Attributes: bus-powered, remote wake-up supported
MaxPower	8	32h	Max current =100mA

Table 5-2 Default Configuration Descriptor

Field	Index	Value	Meaning
bLength	0	09h	Length of the Interface descriptor = 9 bytes
bDescriptorType	1	04h	Descriptor type = interface
bInterfaceNumber	2	00h	Zero based index of this interface = 0
bAlternateSetting	3	00h	Alternate setting =0
bNumEndpoints	4	02h	Number of endpoints in this interface (not counting endpoint0)
bInterfaceClass	5	FFh	Interface Class = vendor specific
bInterfaceSubClass	6	FFh	Interface Sub Class = vendor specific
bInterfaceProtocol	7	FFh	Interface Protocol = vendor specific
Interface	8	00h	Index to string descriptor = none

Table 5-3 Default Interface 0, Alternate Setting 0 Descriptor

Field	Index	Value	Meaning
bLength	0	07h	Descriptor length = 7 bytes long
bDescriptorType	1	05h	ENDPOINT descriptor
bEndpointAddress	2	81h	In endpoint, endpoint #1
bmAttributes	3	02	xfr type = Bulk
wMaxPacketSize(L)	4	20h	Max Packet Size = 32 bytes
wMaxPacketSize(H)	5	00h	
bInterval	6	00h	Polling interval in milliseconds
Field		Value	Meaning
bLength	0	07h	Descriptor length = 7 bytes long
bDescriptorType	1	05h	ENDPOINT descriptor
bEndpointAddress	2	02h	Out endpoint, endpoint #2
bmAttributes	3	02h	xfr type = Bulk
wMaxPacketSize(L)	4	08h	Max Packet Size = 8 bytes
wMaxPacketSize(H)	5	00h	
bInterval	6	00h	Polling interval in milliseconds

Table 5-4 Default Interface 0, Alternate Setting 0, Bulk Endpoint Descriptors

Field	Index	Value	Meaning
bLength	0	04h	String Index 0
bDescriptorType	1	03h	String descriptor type
wLANGID(0)(L)	2	09h	Language ID for English (L)
wLANGID(1)(H)	3	04h	Language ID for English (H)

Table 5-5 String 0 Descriptor

Field	Index	Value	Meaning
bLength	0	26h	String Index 1
bDescriptorType	1	03h	String descriptor type
bString	2	4600h	“Fingerprint Sensor” – in UNICODE format “F”
	4	6900h	“i”, 00
	6	6E00h	“n”, 00
	8	6700h	“g”, 00
	10	6500h	“e”, 00
	12	7200h	“r”, 00
	14	7000h	“p”, 00
	16	7200h	“r”, 00
	18	6900h	“i”, 00
	20	6E00h	“n”, 00
	22	7400h	“t”, 00
	24	2000h	“ “, 00
	26	5300h	“S”, 00
	28	6500h	“e”, 00
	30	6E00h	“n”, 00
	32	7300h	“s”, 00
	34	6F00h	“o”, 00
	36	7200h	“r”, 00

Table 5-6 String 1 Descriptor

A remote wakeup feature supports finger detect while the host has the sensor in the Suspend state. For finger detect wakeup, an internal low power, low frequency oscillator is used to cycle the 12 MHz oscillator on and off, with finger detect attempted whenever the 12 MHz oscillator is enabled. This cycle timing through the Finger Detect Rate register is selectable. Sending a “master reset” command to the sensor will cause a data buffer flush action to occur so any unsent data is made available to the host.

5.3 Reset

The reset input has an internal pull-up of 57K ohm with a tolerance of 30%. A nominal value of 47nF may be used to provide a proper reset to the device. A valid reset is achieved if the reset is still active (less than 2/3 of the VDD rail voltage) for 3 mS after the Vdd voltage has reached the specification limits.

6. SOFTWARE Interface details

The Register Map and bit level Register Descriptions are contained in this section. Reserved registers are not included in the descriptions section for clarity. Bolded text in the register descriptions indicates default functionality.

6.1 Register Map

Reg	D6	D5	D4	D3	D2	D1	D0	Reset
80h	Reserved	Reserved	Reserved	Nav. Mode	OP_Enable	Scan Reset ¹	Master Reset ¹	00h
81h	Reserved	Reserved	Read IDn ¹	Clear One-Shot ¹	Set One-Shot ¹ / One Shot ²	Read Registers ¹	Continuous Scan	00h
82h	Disable Auto Update	Reserved	Demod Blk Dis	Reserved	Reserved	Calibrate Finger Det.	Timer Freerun	04h
83h	Read Ref. Delay	Finger Settling Delay [1]	Finger Settling Delay [0]	Reserved	Detect Rate [2]	Detect Rate [1]	Detect Rate [0]	13h
84h	Reserved	NAV_SEL[1]	NAV_SEL[0]	Nav Corr Range [3] ²	Nav Corr Range [2] ²	Nav Corr Range [1] ²	Nav Corr Range [0] ²	07h
85h	Reserved	Reserved	Nav Fing. Det. Threshold [4]	Nav Fing. Det. Threshold [3]	Nav Fing. Det. Threshold [2]	Nav Fing. Det. Threshold [1]	Nav Fing. Det. Threshold [0]	02h
86h	Reserved	Nav. Reduce LR	Reserved	Nav. Thresh[3]	Nav. Thresh[2]	Nav. Thresh[1]	Nav. Thresh[0]	01h
87h	Reserved	Reserved	Reserved	Reserved	Detect Freq [2]	Detect Freq [1]	Detect Freq [0]	01h
88h	Reserved	Reserved	Reserved	Column Scan Rate [3]	Column Scan Rate [2]	Column Scan Rate [1]	Column Scan Rate [0]	03h
89h	Reserved	Reserved	Measure Square	Reserved	Reserved	Meas Drive [1]	Meas Drive [0]	02h
8Ah	Reserved	Reserved	Reserved	Reserved	Meas Freq [2]	Meas Freq [1]	Meas Freq [0]	05h
8Bh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
8Ch	Demod Phase[13]	Demod Phase[12]	Demod Phase[11]	Demod Phase[10]	Demod Phase [9]	Demod Phase [8]	Demod Phase [7]	40h
8Dh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
8Eh	Reserved	Gain 2 [1]	Gain 2 [0]	Reserved	Reserved	Gain1 [1]	Gain1 [0]	00h
8Fh	Bias2 Unlock	Bias 2 [1]	Bias 2 [0]	Reserved	Bias1 Unlock	Bias 1 [1]	Bias 1 [0]	00h
90h	Carrier Null En	Carrier Null [5]	Carrier Null [4]	Carrier Null [3]	Carrier Null [2]	Carrier Null [1]	Carrier Null [0]	00h
91h	A/D Reference High [6]	A/D Reference High [5]	A/D Reference High [4]	A/D Reference High [3]	A/D Reference High [2]	A/D Reference High [1]	A/D Reference High [0]	70h
92h	A/D Reference Low [6]	A/D Reference Low [5]	A/D Reference Low [4]	A/D Reference Low [3]	A/D Reference Low [2]	A/D Reference Low [1]	A/D Reference Low [0]	20h
93h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
94h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0Ah
95h	Start Col [6]	Start Col [5]	Start Col [4]	Start Col [3]	Start Col [2]	Start Col [1]	Start Col [0]	00h
96h	End Col [6]	End Col [5]	End Col [4]	End Col [3]	End Col [2]	End Col [1]	End Col [0]	7Fh
97h	Low Resolution	Image Res. [1]	Image Res. [0]	Bin. Threshold [3]	Bin. Threshold [2]	Bin. Threshold [1]	Bin. Threshold [0]	08h
98h	Reserved	Test Register Enable	Registers First	Histo Full Array	Reserved	Histo Data Enable	Image Data Disable	20h
99h	Reserved	Reserved	Reserved	GPIO3	GPIO2	GPIO1	GPIO0	00h
9Ah	Power Cycled ²	Scan Paused ²	Finger Present - Timer ²	Scan State [3] ²	Scan State [2] ²	Scan State [1] ²	Scan State [0] ²	XXh
9Bh	Reserved	Reserved	Finger Present - Navigation ²	Challenge Word [31] ¹ / Up ²	Challenge Word [30] ¹ / Down ²	Challenge Word [29] ¹ / Left ²	Challenge Word [28] ¹ / Right ²	00h
9Ch	Challenge Word [27] ¹	Challenge Word [26] ¹	Challenge Word [25] ¹	Challenge Word [24] ¹	Challenge Word [23] ¹	Challenge Word [22] ¹	Challenge Word [21] ¹	00h



Reg	D6	D5	D4	D3	D2	D1	D0	Reset
9Dh	Challenge Word [20] ¹	Challenge Word [19] ¹	Challenge Word [18] ¹	Challenge Word [17] ¹	Challenge Word [16] ¹	Challenge Word [15] ¹	Challenge Word [14] ¹	06h
9Eh	Challenge Word [13] ¹	Challenge Word [12] ¹	Challenge Word [11] ¹	Challenge Word [10] ¹	Challenge Word [9] ¹ /	Challenge Word [8] ¹ / IO_SEL [1] ²	Challenge Word [7] ¹ / IO_SEL [0] ²	0Xh
9Fh	Challenge Word [6] ¹	Challenge Word [5] ¹	Challenge Word [4] ¹	Challenge Word [3] ¹	Challenge Word [2] ¹	Challenge Word [1] ¹	Challenge Word [0] ¹	10h
A0h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	XXh
A1h	Excit Bias Unlock	Manual Excit Bias [1]	Manual Excit Bias [0]	Reserved	Sense Amp Bias Unlock	Sense Amp Bias [1]	Sense Amp Bias [0]	00h
A2h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A3h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A4h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A5h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A6h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A7h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	02h
A8h	Decrease Rdet	Reserved	Reserved	FD Threshold [3]	FD Threshold [2]	FD Threshold [1]	FD Threshold [0]	01h
A9h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
AAh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
ABh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
ACh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Single Reg En	20h
ADh	Single Reg ID [6]	Single Reg ID [5]	Single Reg ID [4]	Single Reg ID [3]	Single Reg ID [2]	Single Reg ID [1]	Single Reg ID [0]	00h
A Eh	Reserved	Reserved	Reserved	Reserved	FDRV X [9]	FDRV X [8]	FDRV X [7]	XXh
A Fh	FDRV X [6]	FDRV X [5]	FDRV X [4]	FDRV X [3]	FDRV X [2]	FDRV X [1]	FDRV X [0]	XXh
B0h	Reserved	Reserved	Watchdog Enable	Reserved	Watchdog Time[2]	Watchdog Time[1]	Watchdog Time[0]	00h
B1h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
B2h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
B3h	Reserved	Reserved	Reserved	GPIO disable [3]	GPIO disable [2]	GPIO disable [1]	GPIO disable [0]	0Fh
B4h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
B5h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
B6h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	26h
B7h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	0Dh
B8h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	6Ch
B9h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
BAh	SOF Timestamp/FreeRun [13] ²	SOF Timestamp/FreeRun [12] ²	SOF Timestamp/FreeRun [11] ²	SOF Timestamp/FreeRun [10] ²	SOF Timestamp/FreeRun [9] ²	SOF Timestamp/FreeRun [8] ²	SOF Timestamp/FreeRun [7] ²	00h
BBh	SOF Timestamp/FreeRun [6] ²	SOF Timestamp/FreeRun [5] ²	SOF Timestamp/FreeRun [4] ²	SOF Timestamp/FreeRun [3] ²	SOF Timestamp/FreeRun [2] ²	SOF Timestamp/FreeRun [1] ²	SOF Timestamp/FreeRun [0] ²	00h
BCh	EOF Timestamp [13] ₂	EOF Timestamp [12] ₂	EOF Timestamp [11] ₂	EOF Timestamp [10] ₂	EOF Timestamp [9] ₂	EOF Timestamp [8] ₂	EOF Timestamp [7] ₂	00h
BDh	EOF Timestamp [6] ₂	EOF Timestamp [5] ₂	EOF Timestamp [4] ₂	EOF Timestamp [3] ₂	EOF Timestamp [2] ₂	EOF Timestamp [1] ₂	EOF Timestamp [0] ₂	00h
BEh	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h

Table 6-1 Registers Summary

¹Write Only
²Read Only

The following sections describe the functional settings for each active Register. Registers which are entirely reserved are not shown in the description sections below.



6.1.1.1 Control Register 1 (CTRL1)

(80h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Nav Mode	Op Enable	Scan Reset	Master Reset
Reset Value	0	0	0	0	0	0	0	0

Nav Mode

- 1 Device will operate in navigation mode, making the contents of register 9Bh valid.
- 0 Device is in imaging mode; contents of register 9Bh are invalid.**

OP Enable

- 1 Imaging or Navigation Mode is enabled.
- 0 Forces idle mode. Clocking is disabled except when enabled by interface activity.**

Scan Reset

- 1 Perform a scan reset. This stops any imaging scan currently in progress and restarts the scan sequencer at recheck for finger present. If an image scan is not in progress, no action is performed. This bit is self-resetting and will always read back as zero.

Master Reset

- 1 Perform a master reset (same as Power On Reset). This resets all registers to their initial values. Output registers and buffer registers are loaded with reset values. This bit is self-resetting and will always read back as zero. This reset does not affect GPIO register settings.

Headings in bold denote default state functionality



6.1.1.2 Control Register 2 (CTRL2)

(81h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Read ID	Clear One-Shot	Set One-Shot	Read Registers	Continuous Scan
Reset Value	0	0	0	0	0	0	0	0

Read ID

1 Read the ID register of the chip. This bit is self-resetting and will always read back as zero.

Clear One-Shot

1 Clears the one-shot flip-flop. This bit is self-resetting and will always read back as zero.

Set One-Shot

1 Set the one-shot flip-flop to allow a single image scan. As soon as the necessary conditions are met (finger present, output buffers empty, output channel ready for data, and finger settling delay expired), an image scan will occur. Note that the Continuous Scan bit must be low for this to have any effect. This bit is self-resetting. The value read for this bit position indicates a single scan is pending. Scan pending can be reset by Scan Reset or Master Reset or by the Clear One-Shot bit.

Read Registers

1 Read the current state of the local registers in the Sensor IC. The request is responded to only if not in Imaging mode. This bit is self-resetting and will always read back as zero.

Continuous Scan

1 Continuous Scan. As long as the necessary conditions are met, image scans will be performed.

0 Controlled Scan. Single scans are initiated by writing a '1' to the Set One-Shot bit.



6.1.1.3 Excitation Common Controls (EXCITCTRL)

(82h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	FD Auto Update Disable	Reserved	Demod Blk Disable	Reserved	Reserved	Calibrate Finger Det.	Timer Free Run
Reset Value	0	0	0	0	0	1	0	0

FD Auto Update Disable

- 1 Disables digital finger detect auto-update function
- 0 Enables digital finger detect auto-update function**

Demod Blk Disable

- 1 Disables option of setting Demod Clock low during DCRSTR.
- 0 Normal operation.**

Calibrate Finger Det..

- 1 Re-calibrate finger detect timer count. Should be done when finger is not on sensor. This bit is self-resetting and always reads back as a '0'.

Timer Free Run

- 1 SOF TIMESTAMP is a free running counter, with lsb changing every 16us.
- 0 SOF TIMESTAMP is updated at start of frame, normal operation.**



6.1.1.4 Detect Control (DETCTRL)

(83h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Read Ref. Delay	Finger Settling Delay [1]	Finger Settling Delay [0]	Reserved	Detect Rate[2]	Detect Rate [1]	Detect Rate [0]
Reset Value	0	0	0	1	0	0	1	1

Read Ref. Delay

- 0** Registers 0xAE and 0xAF read out **FDVR_DELAY**
- 1 Registers 0xAE and 0xAF read out **FDVR_REFERENCE**

Finger Settling Delay

Sets the delay from when Finger On Sensor goes active (and remains active) to when a transition is made to imaging mode.

- 00 16 ms
- 01 32 ms**
- 10 64 ms
- 11 128 ms

Finger Detect Rate [2:0] – Imaging Mode

Sets the rate at which the stimulus source and finger detect circuitry are turned on. For all settings except continuous, the stimulus is turned on for 128 us. The 16mS and 31mS settings get remapped to 62mS in SUSPEND state with the Remote Wakeup feature enabled.

- 000 Detection is continuous.
- 001 Detect cycles occur every 16 msec.
- 010 Detect cycles occur every 31 msec.
- 011 Detect cycles occur every 62 msec.**
- 100 Detect cycles occur every 125 msec.
- 101 Detect cycles occur every 250 msec.
- 110 Detect cycles occur every 500 msec.
- >110 Detect cycles occur every 1 sec.

Finger Detect Rate [2:0] – Navigation Mode

Sets the time in between navigation data packets when in navigation mode.

- 000 Nav. Off time = 4ms (packet spacing 10ms).
- 001 Nav. Off time = 4ms (packet spacing 10ms).
- 010 Nav. Off time = 8ms (packet spacing 14ms).
- 011 Nav. Off time = 16ms (packet spacing 22ms).**
- 1XX Nav. Off time = 32ms (packet spacing 38ms).

6.1.1.5 Navigation Correlation Range (NAVCORRNGE)

(84h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Nav. Select [1]	Nav. Select [0]	Nav. Corr. Range[3]	Nav. Corr. Range[2]	Nav. Corr. Range[1]	Nav. Corr. Range[0]
Reset Value	0	0	0	0	0	1	1	1

Nav. Select[1:0] – Selects mode for determining Up/Down versus Left/Right

00 If the number of excited pixels in the center column is greater than Register 0x85, then Up/Down determination will be made, otherwise make Left/Right determination.

01 If excited pixels in the left, center, and right columns are greater than Register 0x85, then Up/Down determination will be made, otherwise make Left/Right determination.

1X Reserved.

Nav. Corr. Range[3:0]

This register selects the shift range for correlation when in navigation mode and imaging mode for determining shifts to peak correlation. This value limits the number of pixel shifts of the reference images when correlating with the current center column of pixel data. When reference columns are shifted, the fill data is '0', which can in some circumstances cause errors in the correlation data. The default value in this register should be acceptable for most finger data.

6.1.1.6 Navigation Finger Detect Threshold (NAVFDTHRS) (85h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Nav. Fing. Detect Thresh[4]	Nav. Fing. Detect Thresh[3]	Nav. Fing. Detect Thresh[2]	Nav. Fing. Detect Thresh[1]	Nav. Fing. Detect Thresh[0]
Reset Value	0	0	0	0	0	0	1	0

Nav. Fing Detect Thresh[4:0]

Sets the threshold for image based finger detect in navigation mode. It is used to determine if there is a sufficient amount of pixel data in the center column to do up/down direction determination vs. left/right determination. See Register 0x84 for additional options.



6.1.1.7 Navigation Control (NAVCTRL)

(86h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Nav Reduce LR	Reserved	NAV_THRESH [3]	NAV_THRESH [2]	NAV_THRESH [1]	NAV_THRESH [0]
Reset Value	0	0	0	0	0	0	0	1

Nav Reduce LR

Sets location of Left/Right columns for navigation purposes.

- 1 Navigation Left column is at 32, Right column is at 159.
- 0 Navigation Left column is at 16, Right column is at 175.**

NAV_THRESH[3:0]

Sets threshold for image correlation. When ‘Up’ correlation results are compared to ‘Down’ correlation results, the difference between them must be greater than NAV_THRESH in order for a direction answer to be generated. This register is used to adjust correlation sensitivity.



6.1.1.8 Detect Frequency (DETFREQ)

(87h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Detect Freq [2]	Detect Freq [1]	Detect Freq [0]
Reset Value	0	0	0	0	0	0	0	1

Detect Frequency

Sets the frequency of the excitation generator when in Detect mode. Out of range values default to the 2 MHz setting.

- 001 125 KHz**
- 010 250 KHz
- 011 500 KHz
- 100 1 MHz
- 101 2 MHz

6.1.1.9 Column Scan Rate (COLSCAN)

(88h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Column Scan Rate [3]	Column Scan Rate [2]	Column Scan Rate [1]	Column Scan Rate [0]
Reset Value	0	0	0	0	0	0	1	1

Column Scan Rate [3:0]

Sets the time used for scanning one column when using standard Analog Channel circuitry. Out of range settings default to the 2048 us scan period. The time shown in the table for additional data is the time to send the end of frame data (9 bytes authentication word and header plus 64 bytes register data) and assumes the lowest valid baud rate. The Min Baud Rate shown is the lowest baud rate that can be used in gray scale mode (non-packed) without causing scanning to pause. The pixel integration time can be calculated using the equation:

$$\text{Pixel integration time} = \text{Column Rate} - 20\text{us}$$

Value	Column Rate	Image Time
0000	Reserved	
0001	Reserved	
0010	32 us	Required Value for best performance
0011	64 us	
0100	128 us	
0101	256 us	
0110	512 us	
0111	1024 us	
1000	2048 us	
1001	4096 us	
1010	8192 us	
1011	16384 us	
1100	32768 us	
1101	65536 us	
111X	65536 us	



6.1.1.10

Measure Drive (VDCTRLMD) (89h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Measure Square	Reserved	Reserved	Measure Drive [1]	Measure Drive [0]
Reset Value	0	0	0	0	0	0	1	0

Measure Square

1 Selects square wave drive during measure

0 Selects sine wave drive during measure

Measure Drive

Sets the drive level of the excitation generator when using sine wave in Measure mode.

00 0.325 V_{pp}

01 0.65 V_{pp}

10 1.3 V_{pp}

11 2.6 V_{pp}



6.1.1.11

Measure Frequency (MEASFREQ)

(8Ah)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Measure Freq [2]	Measure Freq [1]	Measure Freq [0]
Reset Value	0	0	0	0	0	1	0	1

Measure Frequency

Sets the frequency of the excitation generator when in Detect mode. Out of range values default to the 2 MHz setting.

001	125 KHz
010	250 KHz
011	500 KHz
100	1 MHz
101	2 MHz

For best results, the measurement frequency and column scan rate should be selected so that at least 16 cycles of the measurement frequency occur during the integration time period (see column scan rate).



6.1.1.12

Demod Phase 1(DEMODPHASE1)

(8Ch)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Demod Phase [13]	Demod Phase [12]	Demod Phase [11]	Demod Phase [10]	Demod Phase [9]	Demod Phase [8]	Demod Phase [7]
Reset Value	0	1	0	0	0	0	0	0

Demod Phase

Combined with the next register, Demod Phase 1, these set the phase of the demodulation clock relative to the positive zero crossing of the excitation generator. The bit weighting has the following relative scales:

- Bit[13] – bit weight = 180 degrees
- Bit[7] – bit weight = 2.8125 degrees
- Bit[6] – bit weight = 1.40625 degrees
- Bit[0] – bit weight = 0.02197256 degrees

Default phase is 40h.



6.1.1.13

Channel Gain (CHANGAIN)

(8Eh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Sensor Gain 2 [1]	Sensor Gain 2 [0]	Reserved	Reserved	Sensor Gain 1 [1]	Sensor Gain 1 [0]
Reset Value	0	0	0	0	0	0	0	0

Sensor Gain #2

Sets the gain in the second stage of the analog channel (channel buffer).

00	2x
01	4x
10	8x
11	16x

Sensor Gain #1

Sets the gain in the first stage of the analog channel (array buffer).

00	2x
01	4x
10	8x
11	16x



6.1.1.14

Channel Bias (CHANBIAS)

(8Fh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Bias 2 Unlock	Bias 2 [1]	Bias 2 [0]	Reserved	Bias 1 Unlock	Bias 1 [1]	Bias 1 [0]
Reset Value	0	0	0	0	0	0	0	0

Bias 2 Unlock

Sets the bias current in the second stage of the analog channel (channel buffer).

- 0** **Bias 2 is locked to measure frequency**
- 1 Bias 2 is not locked to measure frequency

Sensor Bias #2

Sets the bias current in the second stage of the analog channel (channel buffer).

- 00** **150 uA**
- 01 300 uA
- 10 600 uA
- 11 1200 uA

Bias 1 Unlock

Sets the bias current in the first stage of the analog channel (array buffer).

- 0** **Bias 1 is locked to measure frequency**
- 1 Bias 1 is not locked to measure frequency

Sensor Bias #1

Sets the bias current in the first stage of the analog channel (array buffer).

- 00** **90 uA**
- 01 180 uA
- 10 360 uA
- 11 720 uA

The total expected analog channel current (IVDDA3) due to these settings is sixteen times the sum of the two currents (the analog channel is sixteen wide).



	D7	D6	D5	D4	D3	D2	D1	D0
	0	Carrier Offset Null Enable	Carrier Offset Null [5]	Carrier Offset Null [4]	Carrier Offset Null [3]	Carrier Offset Null [2]	Carrier Offset Null [1]	Carrier Offset Null [0]
Reset Value	0	0	0	0	0	0	0	0

Carrier Null Enable

- 1 Enables Carrier Null.
- 0 Disables Carrier Null.**

Carrier Offset Null

Adds a negative voltage to the signal prior to the A/D. The table below shows the voltages associated with each setting for a typical V_{CC} of 3.3V. V_{oos} is the DAC output, and the Output Step is the voltage summed with the signal. $V_{step} = 0.103125 * [setting+1]$; based on $V_{dd} = 3.30V$

Value	V_{oos}	Output Step
000000	0.0515625 V	0.0 V
000001	0.103125 V	-0.0515625 V
111110	3.2484375 V	-3.196875V
111111	3.3	-3.2484375V



6.1.1.16

A/D Reference High (ADREFHI)

(91h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	A/D Ref High [6]	A/D Ref High [5]	A/D Ref High [4]	A/D Ref High [3]	A/D Ref High [2]	A/D Ref High [1]	A/D Ref High [0]
Reset Value	0	1	1	1	0	0	0	0

A/D Reference High

Sets the high reference voltage to the A/D converter. The actual voltage reference to the A/D is $(V_{dd}/128) * (\text{setting} + 1)$; based on $V_{dd} = 3.30V$. **[default 70h]**

6.1.1.17

A/D Reference Low (ADREFLO)

(92h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	A/D Ref Low [6]	A/D Ref Low [5]	A/D Ref Low [4]	A/D Ref Low [3]	A/D Ref Low [2]	A/D Ref Low [1]	A/D Ref Low [0]
Reset Value	0	0	1	0	0	0	0	0

A/D Reference Low

Sets the low reference voltage to the A/D converter. The actual voltage reference to the A/D is $(V_{dd}/128) * (\text{setting} + 1)$; based on $V_{dd} = 3.30V$. **[default 20h]**



6.1.1.18

Start Column (STRTCOL)

(95h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Start Column [6]	Start Column [5]	Start Column [4]	Start Column [3]	Start Column [2]	Start Column [1]	Start Column [0]
Reset Value	0	0	0	0	0	0	0	0

Start Column

Sets the starting column for an image scan. The actual starting column is (value*4).

6.1.1.19

End Column(ENDCOL)

(96h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	End Column [6]	End Column [5]	End Column [4]	End Column [3]	End Column [2]	End Column [1]	End Column [0]
Reset Value	0	1	1	1	1	1	1	1

End Column

Sets the ending column for an image scan. The actual ending column is ((value*4) + 3) [or shift the end column value left 2 bits and set the lowers to lsb's to '1' to get the actual end column]. The end column should not be set lower than the start column. Register settings that result in the end column being greater than 191 will select an end column of 191.



	D7	D6	D5	D4	D3	D2	D1	D0
	0	Low Resolution	Image Resolution [1]	Image Resolution [0]	Bin. Threshold [3]	Bin. Threshold [2]	Bin. Threshold [1]	Bin. Threshold [0]
Reset Value	0	0	0	0	1	0	0	0

Low Resolution

1 The values of 4-pixel clusters are averaged together to provide a 250 ppi image. For example, the values from the first two 16-pixel columns yield are averaged in groups of four to provide 8 averaged pixel values

0 Normal operation. Image data is 4-bits per pixel and packed 2 pixels per byte.

Image Resolution [1:0]

00 Image data is 4-bits per pixel and packed 2 pixels per byte.

01 Image data is 1-bit per pixel and packed 8 pixels per byte.

10 Reserved

11 Reserved

Bin. Threshold

Sets the binarization threshold value for 1-bit per pixel mode. Pixels with A/D values greater than or equal to the threshold value are sent as a one. **[default 08h]**



	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Test Register Enable	Registers First	Histo Full Array	Reserved	Histo Data Enable	Image Data Disable
Reset Value	0	0	1	0	0	0	0	0

Test Register Enable

1 Test Registers (Registers with command addresses above 9Fh) are returned with register messages.

0 Test Registers are not returned.

Registers First

1 Registers are returned before image data.

0 Registers are returned after image data.

Histo Full Array

1 The histogram is taken over the full image array.

0 The histogram considers only the center 64x16 pixels.

Histogram Data Enable

1 The histogram message will be sent when imaging.

0 No histogram message is sent when imaging.

Image Data Disable

1 The image data message and authentication message are not returned when imaging.

0 The image data message and authentication word message are returned.

Note: the histogrammer works on raw pixel data.



	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	GPIO3	GPIO2	GPIO1	GPIO0
Reset Value	0	0	0	0	0	0	0	0

Notes on GPIO pins:

1. GPIO pins function as Product ID bits when the USB interface is selected. The Product ID bits are captured at the end of power on reset [when RESET_N transitions from low to high]. When RESET_N is low, the GPIO signal outputs are forced off.
2. With RESET_N inactive, GPIO pins have normal functionality.
3. RESET_N is the only reset state that affects GPIO's and GPIO Output Enables.
4. GPIO pins are affected by power on reset only. Software Master Reset has no effect.

GPIO3

- 1 Sets GPIO3 high.
- 0 Sets GPIO3 low

GPIO2

- 1 Sets GPIO2 high.
- 0 Sets GPIO2 low.

GPIO1

- 1 Sets GPIO1 high.
- 0 Sets GPIO1 low.

GPIO0

- 1 Sets GPIO0 high.
- 0 Sets GPIO0 low.



	D7	D6	D5	D4	D3	D2	D1	D0
	0	Power Cycled	Scan Paused	Finger Present-Timer	Scan State [3]	Scan State [2]	Scan State [1]	Scan State [0]
Reset Value	0	0	0	0	0	0	0	0

READ ONLY

Power Cycled

High indicates the reset input pin has gone active. Cleared after register is read.

Scan Paused

High indicates scan was paused due to input buffer full and unable to accept A/D data. Cleared after the register is read. This bit is also set during histogram messages as the column scan clock is held off to allow the histogram message to complete.

Finger Present-Timer

When high, indicates that finger detect circuitry has determined a finger is on the sensor. The result that is shown is a reflection of the delay based finger detect method.

Scan State

- 0000 Waiting For Finger.
- 0001 In Finger Settling Delay.
- 0010 In Power Up Delay.
- 0011 Waiting To Start Image Scan.
- 0100 Pre-loading Sub array 0.
- 0101 Setup for row advance.
- 0110 Waiting for row advance.
- 0111 Pre-loading Column 0.
- 1000 Setup for column advance.
- 1001 Waiting for column advance.
- 1010 Waiting for Scan Start.
- 1011 Waiting for Scan End.
- 1100 Waiting for Row Setup.
- 1101 Waiting for one column time (depends on scan rate)
- 1110 Waiting for queued data transmission to be completed
- 1111 Wait for 128 us.



6.1.1.24

Challenge Word 1 (CHWORD1)

(9Bh)

	D7	D6	D5	D4	D3	D2	D1	D0
	Reserved	Reserved	Reserved	Reserved / Finger Present - Nav	Challenge Word [31] / Up	Challenge Word [30] / Down	Challenge Word [29] / Left	Challenge Word [28] / Right
Reset Value	0	0	0	0	0	0	0	0

WRITE

Challenge Word [31:28]

Writing to this register alters bits 31 through 28 of the challenge word.

READ

Finger Present-Nav (D4)

- 1 Finger is present – image based finger detect during navigation mode.
- 0 No finger present.

Up/Down/Left/Right (D3:D0)

When Navigation mode is selected, the state of these bits indicate which direction (if a direction is indicated by finger location or movement) the sensor believes the finger is indication for cursor navigation. Values of '0' in all register bits indicate the finger is static.

6.1.1.25

Challenge Word 2 (CHWORD2)

(9Ch)

	D7	D6	D5	D4	D3	D2	D1	D0
	Reserved	Challenge Word [27]/	Challenge Word [26]/	Challenge Word [25]/	Challenge Word [24]/	Challenge Word [23]/	Challenge Word [22]/	Challenge Word [21]/
Reset Value	0	0	0	0	0	0	0	0

WRITE

Challenge Word [27:21]

Writing to this register alters bits 32 through 25 of the challenge word.



6.1.1.26

Challenge Word 3 (CHWORD3)

(9Dh)

	D7	D6	D5	D4	D3	D2	D1	D0
	Reserved	Challenge Word [20]	Challenge Word [19]	Challenge Word [18]	Challenge Word [17]	Challenge Word [16]	Challenge Word [15]	Challenge Word [14]
Reset Value	0	0	0	0	0	1	1	0

WRITE

Challenge Word [20:14]

Writing to this register alters bits 20 through 14 of the challenge word.

6.1.1.27

Challenge Word 4 (CHWORD4)

(9Eh)

	D7	D6	D5	D4	D3	D2	D1	D0
	Reserved	Challenge Word[13]	Challenge Word[12]	Challenge Word[11]	Challenge Word[10]	Challenge Word[9]	Challenge Word[8]/ IO_SEL[1]	Challenge Word[7]/ IO_SEL[0]
Reset Value	0	0	0	0	0	0	1	1

WRITE

Challenge Word [13:7]

Writing to this register alters bits 13 through 7 of the challenge word.

READ

IO_SEL[1:0]

Indicates the selected interface. “11” = USB

6.1.1.28

Challenge Word 5 (CHWORD5)

(9Fh)

	D7	D6	D5	D4	D3	D2	D1	D0
	Reserved	Challenge Word [6]	Challenge Word [5]	Challenge Word [4]	Challenge Word [3]	Challenge Word [2]	Challenge Word [1]	Challenge Word [0]
Reset Value	0	X	X	X	X	X	X	X

WRITE

Challenge Word [6:0]

Writing to this register alters bits 7 through 0 of the challenge word.

Test Register 1 (TREG1)

(A1h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Excit Bias Unlock	Manual Excit Bias[1]	Manual Excit Bias[0]	Reserved	Sense Amp Bias Unlock	Sense Amp Bias[1]	Sense Amp Bias[0]
Reset Value	0	0	0	0	0	0	0	0

Excit Bias Unlock

- 1 Unlocks the controlling of excitation bias as a function of measure frequency.
- 0 Excitation bias changes depending on measure frequency.**

Manual Excit Bias[1:0]

Sets the bias level in the excitation drive circuit.

- 00 0.9 mA**
- 01 1.8 mA
- 10 3.6 mA
- 11 7.2 mA

The table below shows the recommended minimum bias settings based on the highest frequency and drive level being used [assuming a nominal 3.3V power supply].

Frequency	.325 V	.65 V	1.3 V	2.6 V
125 KHz	00b	00b	00b	00b
250 KHz	00b	00b	00b	01b
500 KHz	00b	00b	01b	10b
1 MHz	00b	01b	10b	11b
2 MHz	01b	10b	11b	11b

Sense Bias Unlock

- 1 Unlocks the controlling of sense amp bias as a function of measure frequency.
- 0 Sense amp bias changes depending on measure frequency.**

Sense Amp Bias[1:0]

Selects the bias current of the sense amplifiers.

- 00 2.5 uA**
- 01 5 uA
- 10 8 uA
- 11 10 uA

The table below shows the recommended minimum bias settings based on the measure frequency.

Frequency	
125 KHz	00b
250 KHz	01b
500 KHz	01b
1 MHz	10b
2 MHz	11b



	D7	D6	D5	D4	D3	D2	D1	D0
	0	Decrease Rdet	Reserved	Reserved	FD Threshold [3]	FD Threshold [2]	FD Threshold [1]	FD Threshold [0]
Reset Value	0	0	0	0	0	0	0	1

Decrease Rdet

0 Detect resistor is nominally = 4K ohm.

1 Detect resistor is nominally = 1K ohm.

FD Threshold[3:0]

Sets the Timer-based finger-detect delay threshold. Measured delay values above the setting in this register will cause the FINGER PRESENT condition to be true when using delay based finger detect.



	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Single Reg Enable
Reset Value	0	0	1	0	0	0	0	0

Single Reg. Enable

1 The register read command will produce only 2 bytes, the register address header for the register selected in ADh, and the register contents for that address.

0 **Register read produces full register set at selected interface.**



6.1.1.32

Single Reg. Address (SREGADDR)

(ADh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Single Reg ID [6]	Single Reg ID [5]	Single Reg ID [4]	Single Reg ID [3]	Single Reg ID [2]	Single Reg ID [1]	Single Reg ID [0]
Reset Value	0	0	0	0	0	0	0	0

When reading single register contents is enabled (REG ACh), this register identifies which register address will be read.



6.1.1.33

FDRV X HI (FDRVXHI)

(AEh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	FDRV X[9]	FDRV X[8]	FDRV X[7]
Reset Value	0	0	0	0	0	0	0	0

FDRV X[9:7] READ ONLY

If Register 0x83-D6 = 0 FDRV X = FDRV_DELAY[9:7].

If Register 0x83-D6 = 1 FDRV X = FDRV_REFERENCE[9:7]

6.1.1.34

FDRV X LO (FDRVXLO)

(AFh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	FDRV X[6]	FDRV X[5]	FDRV X[4]	FDRV X[3]	FDRV X[2]	FDRV X[1]	FDRV X[0]
Reset Value	0	0	0	0	0	0	0	0

FDRV X[6:0] READ ONLY

If Register 0x83-D6 = 0 FDRV X = FDRV_DELAY[6:0].

If Register 0x83-D6 = 1 FDRV X = FDRV_REFERENCE[6:0]



6.1.1.35

Watchdog Control (WDCtrl)

(B0h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Watchdog Enable	Reserved	Watchdog Time[2]	Watchdog Time[1]	Watchdog Time[0]
Reset Value	0	0	0	0	0	0	0	0

Watchdog Enable

1 Enables operation of Watchdog timer, which can cause a USB disconnect if the time set in [D2:D0] expires without USB transactions to the sensor.

0 **Normal operation.**

Watchdog Timer[2:0] – Selects timeout value for watchdog timer. Required settings for system use are 2 seconds or above

000	15 ms
001	100ms
010	500ms
011	1 second
100	2 seconds
101	3 seconds
110	4 seconds
111	5 seconds



	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	GPO disable [3]	GPO disable [2]	GPO disable [1]	GPO disable[0]
Reset Value	0	0	0	0	1	1	1	1

GPIO3 Disable

- 1 GPIO3 output is disabled, pin may be used as an input.**
- 0 GPIO3 pin is an output.

GPIO2 Disable

- 1 GPIO2 output is disabled, pin may be used as an input.**
- 0 GPIO2 pin is an output.

GPIO1 Disable

- 1 GPIO1 output is disabled, pin may be used as an input.**
- 0 GPIO1 pin is an output.

GPIO0 Disable

- 1 GPIO0 output is disabled, pin may be used as an input.**
- 0 GPIO0 pin is an output.



6.1.1.37

SOF Timestamp/FreeRun[13:7] (SOFTIMEHIGH)

(BAh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	SOF Timestamp [13]	SOF Timestamp [12]	SOF Timestamp [11]	SOF Timestamp [10]	SOF Timestamp [9]	SOF Timestamp [8]	SOF Timestamp [7]
Reset Value	0	0	0	0	0	0	0	0

SOF Timestamp/Free Run[13:7] READ ONLY

This register indicates the upper 7 bits of the start of imaging timestamp. When Register 0x82-D0 is set, the counter free runs and these bits are updated at the time of the register read.

6.1.1.38

SOF Timestamp/FreeRun[6:0] (SOFTIMELOW)

(BBh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	SOF Timestamp [6]	SOF Timestamp [5]	SOF Timestamp [4]	SOF Timestamp [3]	SOF Timestamp [2]	SOF Timestamp [1]	SOF Timestamp [0]
Reset Value	0	0	0	0	0	0	0	0

SOF Timestamp/FreeRun[6:0] READ ONLY

This register indicates the lower 7 bits of the start of imaging timestamp. When Register 0x82-D0 is set, the counter free runs and these bits are updated at the time of the register read.

6.1.1.39

EOF Timestamp[13:7] (EOFTIMEHIGH)

(BCh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	EOF Timestamp [13]	EOF Timestamp [12]	EOF Timestamp [11]	EOF Timestamp [10]	EOF Timestamp [9]	EOF Timestamp [8]	EOF Timestamp [7]
Reset Value	0	0	0	0	0	0	0	0

EOF Timestamp[13:7] READ ONLY

This register indicates the upper 7 bits of the end of imaging timestamp. This is a free running counter.



6.1.1.40

EOF Timestamp[6:0] (EOFTIMELOW)

(BDh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	EOF Timestamp [6]	EOF Timestamp [5]	EOF Timestamp [4]	EOF Timestamp [3]	EOF Timestamp [2]	EOF Timestamp [1]	EOF Timestamp [0]
Reset Value	0	0	0	0	0	0	0	0

EOF Timestamp[6:0] READ ONLY

This register indicates the lower 7 bits of the end of imaging timestamp. This is a free running counter.

7. Data Formats

7.1 Overview

The sensor communicates with the host via data packets. A one-byte header that identifies the message precedes each data packet type. Note that since the pixel data formats use all 8-bits per byte, the header bytes are not unique in the data stream. Software can use the header bytes to verify that it is synchronized with the data stream. They cannot be used as a mechanism to synchronize with the data. If software gets out of synch with the data, it should disable image scanning and issue a scan reset. This will cause the data stream to stop. The following table shows the header byte definitions for each message type.

Header Byte	Definition
80h – BEh	Register headers
BFh – DDh	Reserved.
DEh	Precedes 32 byte histogram message.
DFh	Precedes eight byte authentication value.
E0h	Precedes 500 ppi array data message in gray scale. The array message is 192 columns x 16 pixels per column x ½ byte per pixel = 1536 bytes. In 250 ppi mode, the array message is 96 columns x 8 pixels per column x ½ byte per pixel = 384 bytes. In Extended Precision 250 ppi mode, the array message is 96 columns x 8 bytes per column = 768 bytes.
E1h-EFh	Reserved
F0h	Precedes array data message in binary mode. The array message is 192 columns x 16 pixels per column x 1/8 byte per pixel = 384 bytes. In 250 ppi Mode, the array message is 96 columns x 8 pixels per column x 1/8 byte per pixel = 96 bytes.
F1h –FFh	Reserved.

Table 7-1 Command Byte Definition

7.1.1 Registers Message Format

When a request to read registers is received (initiated by setting the Read Registers bit in Register 81h-D1, all of the register values are returned preceded by the header for that register.

Registers are written to by writing the register ID followed by the data byte.

7.1.2 Image Data Format – Grey Scale 500 ppi

Table 7-2 shows the image data format in this mode.

Byte	Data (D7 – D0)
1	Header (E0h)
2	Column 1 pixel 2[3:0], Column 1 pixel 1[3:0]
3	Column 1 pixel 4[3:0], Column 1 pixel 3[3:0]
4	Column 1 pixel 6[3:0], Column 1 pixel 5[3:0]
5	Column 1 pixel 8[3:0], Column 1 pixel 7[3:0]
6	Column 1 pixel 10[3:0], Column 1 pixel 9[3:0]
7	Column 1 pixel 12[3:0], Column 1 pixel 11[3:0]
8	Column 1 pixel 14[3:0], Column 1 pixel 13[3:0]
9	Column 1 pixel 16[3:0], Column 1 pixel 15[3:0]
10	Column 2 pixel 2[3:0], Column 1 pixel 1[3:0]
1537	Column 192 pixel 16[3:0], Column 192 pixel 15[3:0]

Table 7-2 Gray Scale Message Format

The 0xE0h header for the row is sent first, followed by each column vector sent as eight bytes. The 64-bit pixel data also updates the authentication word. After all data for the selected number of rows is sent, the authentication word is sent preceded by the header byte for the authentication message. The authentication data is sent lower byte first. The register values are then returned, with each register preceded by the command byte for the register. The register values are the ones that were in effect during the image.

7.1.3 Image Data Format – 250 ppi

Table 7-3 shows the image data format for this mode.

Byte	Data (D7 – D0)
1	Header (E0h)
2	Col 1/Col 2 pixel group 1 [3:0], Col 1/Col 2 pixel group 2 [3:0]
3	Col 1/Col 2 pixel group 3 [3:0], Col 1/Col 2 pixel group 4 [3:0]
4	Col 1/Col 2 pixel group 5 [3:0], Col 1/Col 2 pixel group 6 [3:0]
5	Col 1/Col 2 pixel group 7 [3:0], Col 1/Col 2 pixel group 8 [3:0]
6	Col 3/Col 4 pixel group 1 [3:0], Col 3/Col 4 pixel group 2 [3:0]
385	Col 191/Col 192 pixel group 7 [3:0], Col 191/Col 192 pixel group 8 [3:0]

Table 7-3 4 Bit 250 ppi Gray Scale Message Format

The header for the row is sent first, followed by each 2-column vector sent as eight bytes. The difference between this mode and 500 ppi mode is that four adjacent pixels are summed together and returned as a single 4-bit value. The 64-bit pixel data updates the authentication word in the same format as for normal data. After all data for the selected number of columns is sent, the authentication word is sent preceded by the header byte for the authentication message. The authentication data is sent lower byte first. The register values are then returned, with each register preceded by the command byte for the register. The register values are the ones that were in effect during the image.

7.1.4 Image Data Format – Monochrome

The packed monochrome data format sends only a one bit value per pixel but packs the data so all eight bits are used. Table 7-4 shows the data format in this mode.

Byte	Data (D7 – D0)
1	Header (F0h)
2	Column 1 pixels 8-1
3	Column 1 pixels 16-9
4	Column 2 pixels 8-1
5	Column 2 pixels 16-9
385	Column 192 pixels 16-9

Table 7-4 Monochrome Packed Message Format

The header for the row is sent first, followed by each column sent as two bytes. The 64-bit value from four columns updates the authentication word in the same manner as for normal data. After all data for the selected number of rows is sent, the authentication word and register data are sent as in normal mode.



7.1.5 Histogram Message Format

When the histogram message is enabled, it is sent once per image. When sent once per image, it will be sent after the image data and before the authentication word. The histogram message is preceded by a header byte (0xDE). The header is followed by the counts for each of the bins representing possible pixel values. Bin 0 (the number of pixels whose value is 0) is sent first as two bytes. The first byte has the lower seven bits and the second byte has the upper seven bits. This is followed by the counts for the remaining bins

Byte	Data (D6 – D0)
1	Header (0xDE)
2	Bin0[6:0]
3	Bin0[13:7]
4	Bin1[6:0]
5	Bin1[13:7]
6	Bin2[6:0]
32	Bin15[6:0]
33	Bin15[13:7]

Table 7-5 Histogram Message Format

7.1.6 Authentication Word Message Format

The authentication word is sent after an image is complete. The authentication word message is preceded by a header byte (0xDF). The authentication word is used to validate that the transaction is authentic (i.e. that the image data isn't being provided from some storage device containing a valid fingerprint image).

Byte	Data (D6 – D0)
1	Header (0xDF)
2	Authentication Word [7:0]
3	Authentication Word [15:8]
4	Authentication Word [23:16]
5	Authentication Word [31:24]
6	Authentication Word [39:32]
7	Authentication Word [47:40]
8	Authentication Word [55:48]
9	Authentication Word [63:56]

Table 7-6 Authentication Word Message Format

8. Part Numbering Scheme

AES2501A – I – PP – CC – DDEE

I = Temperature Range

C = Commercial temperature range = 0C to + 70C

PP = Packaging Options

GA = 48 BGA with std. Leaded Balls

GF = 48 BGA with lead free Balls

CC = Carrier Options

CA = Plastic Carrier Trays 240 sensors per tray

TR = Tape & Reel w/ 3500 sensors per reel

DD = Drive Ring Options:

GO = Gold

NI = Nickel

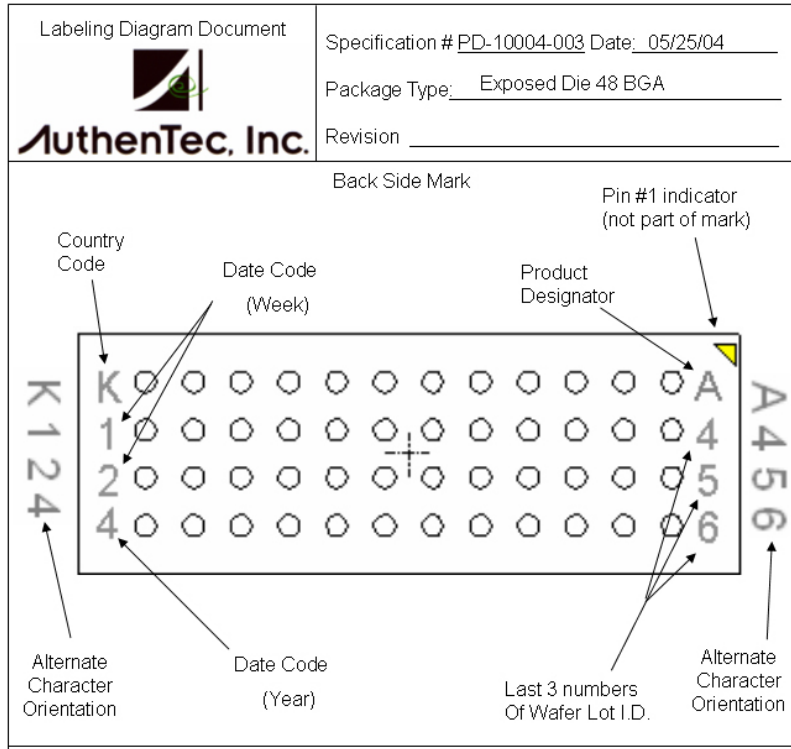
EE = Options

0A = Silicon revision code in 2501A series*

* Contact AuthenTec Sales for current revision code.

Example: AES2501A with Gold ring, Lead-free solder balls, shipped as tape reels:
AES2501A-C-GF-TR-GO0A

Package Backside Laser Part Marking



Date Code Legend:

Ink Color: Laser Marking

K = Country Code (U=USA, K=Korea, T=Taiwan, S= Singapore, C= China)

124 = Mold Week & Year (example shown: week 12, year 2004)

A = Product Designator : E= ES2501A Pb-Free; R= AES2501A with Pb

456 = Wafer Lot I.D. from manufacturer

9. Revision History

Version	Date	Person	Reason
Released	12/29/03	Lee	Release Date of Public Specification
1.1	30 March 04	Lee	Added power supply ripple spec.
1.2	30 May 04	Lee	Formatting Fixes...
1.3	10 Aug 04	Lee	Added part numbering and backside laser mark info
1.0	28 Oct 04	Lee	Updates for 2501A – A10 Pin change to PLL_FILTER Pin change necessitates new part number. PID Update, Pin 1 Marking data, Register B0 change,
1.1	17 Nov 04	Lee	Updated Reset Register Values