A-285-MRC Fingerprint Module

Features
- 2D capacitive fingerprint area sensor
- Sensor array of 288 by 208 pixels
- 508 DPI spatial resolution
- 8-bit pixel value / 256 gray levels
- 14.4 mm x 10.4 mm active sensing area
- High speed SPI interface
- Image capture speed up to 2 MPixel/sec
- ESD protection : + / - 15kV (Air mode)
- Low power : Normal and Standby modes
- > 30 million finger placements
- FPC connection interface

Overview
A-285-MRC integrates the most advanced capacitive sensing technology and packaging process available today. The advantages include high image quality, low power consumption, robust coating material, 15kV ESD protection, adaptability to wide range of temperature, straightforward SPI interface through an 8-pin flexible cable connection.

Table 1 / Brief facts

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage (Vdd)</td>
<td></td>
<td>2.7</td>
<td>3.0</td>
<td>3.3</td>
<td>Volt</td>
</tr>
<tr>
<td>Supply current (Idd)</td>
<td>Vdd=2.7V</td>
<td></td>
<td>2.9</td>
<td>3.3</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>Vdd=3.3V</td>
<td></td>
<td>3.1</td>
<td>3.5</td>
<td>mA</td>
</tr>
<tr>
<td>Active area</td>
<td></td>
<td>14.4</td>
<td>10.4</td>
<td></td>
<td>mm²</td>
</tr>
<tr>
<td>Spatial resolution</td>
<td></td>
<td>508</td>
<td></td>
<td></td>
<td>DPI</td>
</tr>
<tr>
<td>Pixel resolution</td>
<td></td>
<td>8</td>
<td></td>
<td></td>
<td>bit</td>
</tr>
<tr>
<td>Operating temperature</td>
<td></td>
<td>-30</td>
<td>80</td>
<td></td>
<td>ºC</td>
</tr>
<tr>
<td>Storage temperature</td>
<td></td>
<td>-40</td>
<td>85</td>
<td></td>
<td>ºC</td>
</tr>
<tr>
<td>Dimension</td>
<td></td>
<td>33.40</td>
<td>20.40</td>
<td>2.33</td>
<td>mm</td>
</tr>
</tbody>
</table>
The slave mode SPI interface with the operation mode CPHA=0 and CPOL=0. The maximum clock rate is 32Mhz. For the command and data protocol, refer to the A-series Fingerprint Sensor Programming Manual.
Electrical characteristics

Table 3 / Operation mode (-30°C~80°C)

<table>
<thead>
<tr>
<th>Name</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vdd</td>
<td>Supply voltage (Vdd)</td>
<td></td>
<td>2.7</td>
<td>3.0</td>
<td>3.3</td>
<td>Volt</td>
</tr>
<tr>
<td>Idd</td>
<td>Supply current (Idd)</td>
<td>Vdd=2.7V</td>
<td>2.9</td>
<td>3.3</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Vdd=3.3V</td>
<td>3.1</td>
<td>3.5</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

Digital input and outputs

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Condition</th>
<th>Min.</th>
<th>Typ.</th>
<th>Max.</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIL</td>
<td>Input logic low level</td>
<td></td>
<td></td>
<td>0.25Vdd</td>
<td>Volt</td>
<td></td>
</tr>
<tr>
<td>VIH</td>
<td>Input logic high level</td>
<td>0.75Vdd</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cin</td>
<td>Input capacitance</td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>VIL</td>
<td>Output logic low level</td>
<td>Max@4mA</td>
<td>0.2</td>
<td></td>
<td>0.5</td>
<td>Volt</td>
</tr>
<tr>
<td>VOH</td>
<td>Output logic high level</td>
<td>Min@1mA</td>
<td>Vdd-0.3</td>
<td></td>
<td>Vdd-0.2</td>
<td>Volt</td>
</tr>
<tr>
<td>Ileak</td>
<td>Idle leakage current</td>
<td><a href="mailto:Vdd@3.0V">Vdd@3.0V</a></td>
<td>2</td>
<td></td>
<td></td>
<td>uA</td>
</tr>
<tr>
<td></td>
<td></td>
<td><a href="mailto:Vdd@2.7V">Vdd@2.7V</a></td>
<td>4</td>
<td></td>
<td></td>
<td>uA</td>
</tr>
</tbody>
</table>

Table 4 / Absolute maximum ratings

<table>
<thead>
<tr>
<th>Parameter</th>
<th>value</th>
<th>unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating temperature</td>
<td>-30~80</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>-40~85</td>
<td>°C</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>0~3.5</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage</td>
<td>-0.5~Vdd+0.5</td>
<td>V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>-0.5~Vdd+0.5</td>
<td>V</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>9</td>
<td>mW</td>
</tr>
<tr>
<td>ESD on IO pads</td>
<td>±2</td>
<td>kV</td>
</tr>
<tr>
<td>ESD on sensing area (Air)</td>
<td>±15</td>
<td>kV</td>
</tr>
<tr>
<td>ESD on sensing area (Mach)</td>
<td>±7</td>
<td>kV</td>
</tr>
<tr>
<td>ESD on metal bezel (Mach)</td>
<td>±8</td>
<td>kV</td>
</tr>
</tbody>
</table>
### Table 5 / Environmental performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Reference</th>
<th>Condition</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cold operational</td>
<td>IEC60068-2-1 Ab</td>
<td>72h</td>
<td>-30</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Hot operational</td>
<td>IEC60068-2-1 Bb</td>
<td>72h</td>
<td></td>
<td>+80</td>
<td>°C</td>
</tr>
<tr>
<td>Cold storage</td>
<td>IEC60068-2-1 AB</td>
<td>16h</td>
<td>-40</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td>Temperature cycling</td>
<td>IEC60068-2-14 Na</td>
<td>1h/1h 25cycles</td>
<td>-40</td>
<td>100</td>
<td>°C</td>
</tr>
<tr>
<td>Humid heat</td>
<td>IEC60068-2-67 Cy</td>
<td>85°C/85%RH</td>
<td></td>
<td>168</td>
<td>hour</td>
</tr>
<tr>
<td>Other</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Waterproof</td>
<td>IEC60529 IP65</td>
<td>25°C/65%RH</td>
<td>2</td>
<td></td>
<td>hour</td>
</tr>
<tr>
<td>Q-UV test</td>
<td>IEC60068-2-5 Sa</td>
<td>0.63W/m² @55°C</td>
<td>60</td>
<td></td>
<td>hour</td>
</tr>
</tbody>
</table>

### Table 6 / Coating durability tests

<table>
<thead>
<tr>
<th>Test</th>
<th>Result</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pencil hardness test / 750g</td>
<td>&gt; 7H</td>
</tr>
<tr>
<td>RCA Abrasion wear test</td>
<td>&gt; 700 cycles</td>
</tr>
</tbody>
</table>

### Table 7 / Flex Cable Recommendation

<table>
<thead>
<tr>
<th>pitch</th>
<th>Thickness</th>
</tr>
</thead>
<tbody>
<tr>
<td>1± 0.08mm</td>
<td>0.3± 0.05mm</td>
</tr>
</tbody>
</table>
Application information

To achieve the best performance with minimum noise interference, the flat cable connection should be restricted to 25cm. Shielding should be considered when the spacial arrangement involves other active elements, such as power supply, in the system.

ESD discharge pads are provided on the back side of the PCB, located at the 4 corner and alone the longer edge.

![Image of PCB with ESD discharge pads marked]

It is required to provide a low-impedance conductive path from the ESD discharge pads, preferably all of them, to the system chassis or earth ground.

To protect the IO pins connecting to the main processor, it is recommended to use an ESD protection device on each signal wire. For convenience, a 4-in-1 bidirectional device such as AZC199-04SC can be used.

![Diagram of Sensor module to Processor board with ESD protection device]
The A285-MRC sensor module provides two operation modes: basic (passive) mode and active (enhanced imaging) mode. The active mode requires the metal bezel to be used as a source for transmitting a low voltage excitation signal to the touching finger. To avoid unwanted attenuation of the excitation signal, the metal bezel should be insulated from any conductive mounting structure, possibly via a non-conductive gasket.

The internal circuitry of the sensor is well protected by the built-in TVS devices. The metal bezel is also isolated to the driving source via a series resistor and TVS. It is usually underestimated that the signal and power connection between the sensor module and the processor board could be damaged by ESD discharge. It is suggested to add TVS device and possibly series resistor (such as 100 ohm) or inductor (ferrite bead) for each signal line. And on top of it, it is strongly recommended to provide a solid, low impedance connection between the module ESD pad to the system/processor ESD shield or exit, such as earth ground.
Product naming / ordering information

A-prod-code-Aaa Bb C D ee

prod : product code
365, 285, 192, 172, 162, 122
code : packaging identifiers
M - sensor only
P - sensor with processor
F - flat surface with buried metal bezel
R - exposed metal bezel
E - embedded process
C - flat cable connector
Q - QFN/LGA style pads
Aaa : coating
A  N - no coating
K  black
W  white
T  transparent
aa 00 - no coating
   01 - matte
   02 - semi glossy
   03 - glossy
   04 - transparent
   05-99 - serialized version
Bb : PCB version
B  A~Z - version
   b  0~Z - sub-version
C : bezel version
   0  no bezel
   1~Z - version
D : grade code
   0  grade 0
   1  grade 1
ee : serial number
Programming Guide

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1.0 Hardware overview

The following block diagram represents the system in a firmware point of view.

All control and data exchange functions are performed through the SPI interface (described in 2.1). The build-in clock oscillator provides Control Logic a basic timing reference. The Control Logic block generates timing signals necessary for the Sensing Array, which produces varying voltage signal according to the valley and ridge of finger surface. The analog circuit AMP amplifies the weak fingerprint signal. The ADC (Analog-to-digital converter) circuitry further digitize the amplified fingerprint signal.

The digitized fingerprint image signal can be encrypted, or passed directly to the Data Buffer, and get ready to be transferred to the host processor through the SPI interface.

2.0 The A-series command and registers

The A-series operation is controlled by sending commands and receiving through the SPI interface. The A-series SPI interface follows the standard SPI protocol with CPHA=0 and CPOL=0 (refer to http://en.wikipedia.org/wiki/Serial_Peripheral_Interface_Bus for the detail of CPHA and CPOL mode definition).

There are several SPI command codes for controlling A-series:
The control registers are summarized as below:

<table>
<thead>
<tr>
<th>N</th>
<th>name</th>
<th>function</th>
<th>RW</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>reg0</td>
<td>clock control</td>
<td>RW</td>
<td>x90</td>
<td>DETDIV(0011)</td>
<td>OSCDIV(0000)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>reg1</td>
<td>timing paern</td>
<td>RW</td>
<td>x00</td>
<td>RSTT(0000)</td>
<td>SAMPT(0000)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>reg2</td>
<td>analog tuning</td>
<td>RW</td>
<td>x54</td>
<td>ADC_ISEL(001)</td>
<td>PGA_ISEL(001)</td>
<td>BG_ISEL(001)</td>
<td>ADREF</td>
<td>LDOSUS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>reg3</td>
<td>analog tuning</td>
<td>RW</td>
<td>x99</td>
<td>PSF_ISEL(001)</td>
<td>SF_ISEL(001)</td>
<td>VOOR_ISEL(10)</td>
<td>OSC_ISEL(001)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>reg4</td>
<td>analog tuning+detect</td>
<td>RW</td>
<td>x93</td>
<td>SELI(001)</td>
<td>SELR(001)</td>
<td>VODESEL(011)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>reg5</td>
<td>offset</td>
<td>RW</td>
<td>x90</td>
<td>ADCO (0)</td>
<td>OFFS(1000000)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>reg6</td>
<td>analog options + gain</td>
<td>RW</td>
<td>x94</td>
<td>[reserved]</td>
<td>ACONF(000)</td>
<td>PGAGAIN(010)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>reg7</td>
<td>timing paern</td>
<td>RW</td>
<td>x90</td>
<td>SCANDelay(0011)</td>
<td>CDSKPN(0000)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>reg8</td>
<td>finger detection</td>
<td>RW</td>
<td>x96</td>
<td>DETCUP(10)</td>
<td>DETTH(000110)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>9</td>
<td>reg9</td>
<td>I/O/4M control</td>
<td>RW</td>
<td>x24</td>
<td>[reserved]</td>
<td>TRIM(1000)</td>
<td>TRIM2(100)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>reg10</td>
<td>T1/T2 port config</td>
<td>RW</td>
<td>x00</td>
<td>INVIO1(0)</td>
<td>LTEST(0)</td>
<td>T2SEL(00)</td>
<td>T2E(0)</td>
<td>T2SEL(00)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>reg11</td>
<td>control bits</td>
<td>RW</td>
<td>x00</td>
<td>SUBS(0)</td>
<td>INVIMGI(0)</td>
<td>END(0)</td>
<td>ENCRYI</td>
<td>ENPWR</td>
<td>ENADC</td>
<td>EN1K</td>
</tr>
<tr>
<td>12</td>
<td>reg12</td>
<td>option and enable chip</td>
<td>RW</td>
<td>x00</td>
<td>[reserved]</td>
<td>RSTPAT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>13</td>
<td>reg13</td>
<td>OTP address</td>
<td>W</td>
<td>x00</td>
<td>OTPADR</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>14</td>
<td>reg14</td>
<td>OTP data data</td>
<td>W</td>
<td>x00</td>
<td>OTPWD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>reg15</td>
<td>OTP command</td>
<td>W</td>
<td>x00</td>
<td>PROG</td>
<td>NVSTR</td>
<td>AE</td>
<td>CE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>16</td>
<td>reg16</td>
<td>HSI2E</td>
<td>R</td>
<td>x6F</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>17</td>
<td>reg17</td>
<td>VSI2E</td>
<td>R</td>
<td>x6F</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>reg18</td>
<td>ID</td>
<td>R</td>
<td>x14</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>19</td>
<td>reg19</td>
<td>ID</td>
<td>R</td>
<td>x52</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### 2.1 The SPI command protocol

Command and data are exchanged through the SPI MISO and MOSI wires. Each byte of data sent through the MOSI port brings back a received byte through the MISO port.

Commands can be cascaded one by another. The term “SPI command sequence” in the following context is defined as a sequence of command code and data bytes exchanged within one low (active) SPISEL(SSEL) strobe.

The SPI interface timing are summarized in the following figure:
### Symbol | Parameter | Min  | Typ  | Max  
---|---|---|---|---
| tc  | SCLK cycle time* | 31 ns |  |  
| ta  | Data out access time | 4 ns |  | 15 ns  
| tsu | Data in set up time | 2.5 ns |  |  
| thd | Data in hold time | 4 ns |  |  
| tv  | Data out valid time | 16 ns |  | 22 ns  

* Maximum SCLK frequency is 32Mhz

An A-series command code may or may not have associated data. The “start_scan” and “srst” commands don’t have associated data, and will take effect immediately after the command code is sent.

For read/write data commands, the second byte will be the beginning of data byte or bytes, as illustrated below:

**read command**

<table>
<thead>
<tr>
<th>read command</th>
<th>next command</th>
</tr>
</thead>
</table>

| result of previous cmd | return data |

**write command**
Writing and reading a series of register content may look different. For writing to consecutive registers, an internal address counter is incremented automatically after each byte written. This mechanism eliminates the need to repeat sending the 0x40+N command for each register. The sequence of read/write commands may look like the following.

**read sequence (the last command byte is a dummy command)**

**write sequence**

**read image sequence**

In fact, except for the write register command (which writes a sequence of register content), commands can be mixed in a single sequence like following:
2.2 Command code detail

**Code 01 - start scan command**

This command starts the internal fingerprint capture sequence. This is write-only command.

**Code 02 - read pixel data command**

This command reads the first available fingerprint data byte from FIFO.

**Code 03 - read status**

This command returns an internal status byte, which encodes the following information:

<table>
<thead>
<tr>
<th>Bit</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 (LSB)</td>
<td>buffer is empty</td>
</tr>
<tr>
<td>1</td>
<td>buffer is half full</td>
</tr>
<tr>
<td>2</td>
<td>buffer is almost full</td>
</tr>
<tr>
<td>3</td>
<td>internal fault</td>
</tr>
<tr>
<td>4</td>
<td>scan in progress</td>
</tr>
<tr>
<td>5</td>
<td>finger detect interrupt</td>
</tr>
<tr>
<td>6</td>
<td>finger detect in progress</td>
</tr>
<tr>
<td>7 (MSB)</td>
<td>scan is done</td>
</tr>
</tbody>
</table>

**Code 04 - initialize OTP**

This command prepares OTP for operation. For encrypted data transfer, this command also loads the encryption keys from OTP to the encryption module. When issuing this command, the internal clock oscillator must be enabled.

**Code 05 - push a random byte into data FIFO**
This command forces an unpredictable random data byte to be pushed into the data FIFO. This command is used to enhance data security in the encrypted data transfer mode.

**Code 06 - strobes the internal OTP address enable signal**

This command is used during OTP operation (see section 4.2 for detail).

**Code 07 - OTPRD**

This command reads OTP content addressed by current OTP address register.

**Code C1 (decimal 193) - software reset**

This command produces a software reset to all the internal state machines and force them into idle state. This command does not restore the control registers to default value like the hardware reset does.

**Code 20+N - register read command**

This command reads the content of register N. A second byte exchange is required to receive the read data.

**Code 40+N - register write command**

This command starts register write sequence starting at address N. The first byte is the command code, followed by the single or multiple bytes to be written to the registers.

### 2.3 Register detail

**Reg0 / Clock control**

- DETDIV (4bit) - divider for detection clock
- OSCDIV (4bit) - divider for the main oscillator

**Reg1 / Sample timing control**

- RSTT (4bit) - reset timing for each scan line
- SAMPT (4bit) - sample timing for each scan line

**Reg2 / ADC setting 1**

- ADC_ISEL (2bit) - ADC parameter
- PGA_ISEL (2bit) - AMP parameter
- BG_ISEL (2bit) - Bandgap voltage control parameter
- ADCREF (1bit) - ADC reference option (set to 1 to reduce ADC range)
- LDOSUS (1bit) - Reference voltage option

Reg3 / ADC setting 2
- PSF_ISEL (2bit) - ADC parameter
- SF_ISEL (2bit) - ADC parameter
- VDDR_ISEL (2bit) - Reference voltage parameter
- OSC_ISEL (2bit) - Clock oscillator control parameter

Reg4 / Clock oscillator setting
- SELI (2bit) - Clock oscillator design option
- SELR (2bit) - Clock oscillator design option
- VDETSEL (4bit) - Reference voltage select for finger detect

Reg5 / Offset
- ADCIOPT (1bit) - ADC design option
- ADCOFFS (7bit) - ADC offset

Reg6 / Gain
- bit7~6 - (reserved)
- ACONF(3bit) - analog test options (not used)
- PGAGAIN (3bit) - amplifier gain setting

Reg7 / Delay and offset
- SCANDELAY (4bit) - delay for scan start for each line
- CDSCPN (4bit) - sampling compensation parameter

Reg8 / Finger detection control
- DETCLK (2bit) - finger detection clock selection
- DETTH (6bit) - finger detection threshold

Reg9 / Oscillator control
- bit7~6 - (reserved)
- TRIM6K (3bit) - trim sleep clock
- TRIM4M (3bit) - trim main oscillator

Reg10 / IO control bits (see section 4.3)
- INVIO1 (1bit) - invert T1 output
- LTEST (1bit) - logic test mode
- T1SEL (2bit) - T1 function select
- INVIO2 (1bit) - invert T2 output
- T2OE (1bit) - enable T2 output
- T2SEL (2bit) - T2 function select

**Reg11 / Control bits**

- SUBSCAN (1bit) - enable subsampling (1 out of 4 column/row) mode
- INVIMG (1bit) - invert image
- ENDET (1bit) - enable detect mode
- ENCRYP (1bit) - enable encryption mode
- ENPWR (1bit) - enable power circuitry
- ENADC (1bit) - enable analog circuit
- EN6K (1bit) - enable sleep clock
- EN4M (1bit) - enable main oscillator

**Reg12 / Mode control bits**

- bit7~5 - (reserved)
- RSTPAT (5bit) - enable code

**Reg13 / OTP address (see section 4.2)**

- OTPADR (bit [4:0]) - the OTP address register

**Reg14 / OTP write data (see section 4.2)**

- OTPWD (8bit) - the OTP write data

**Reg15 / OTP control bits (see section 4.2)**

- PROG (bit 7)
- NVSTR (bit 6)
- AE (bit 1)
- OE (bit 0)

**Reg16 / Array width (Read only)**

- Returns the width of sensing array (divided by 2 and minus 1)

**Reg17 / Array height (Read only)**

- Returns the height of sensing array (divided by 2 and minus 1)
Reg30 / Chip ID (High byte, read only)

- Returns the chip ID (high byte)

Reg31 / Chip ID (Low byte, read only)

- Returns the chip ID (low byte)

### 2.4 Flow control

As the fingerprint image is being captured and saved in the on-chip buffer memory, the buffer memory overflow or underflow may happen if there is a mismatch of image capture speed and SPI data transfer rate. To avoid buffer overflow, the internal logic stops the image sampling process when the buffer memory is almost full, and resumes operation when the buffer space becomes available.

Buffer underflow is handled differently in the non-encrypted and the encrypted modes. For non-encrypted mode, the data code 255 (0xff) is simply used to encode buffer empty status, while valid image data values are from 0 to 254. For encrypted data transfer, all the 256 codes from 0 to 255 are valid data. In this case buffer underflow can be handled by either using a SPI transfer (clock) speed that is slower than the data sampling rate, or regularly checking the buffer status.

The buffer status bits in the Status register represents the following condition:

- Buffer is empty (bit0): The buffer memory is empty
- Buffer is half-full (bit1): The buffer memory contains more than 10 bytes of data
- Buffer is almost-full (bit2): The buffer memory contains more than 14 bytes of data

### 3.0 Operation

#### 3.1 General description

The A-series hardware design implements a finger detection scheme that allows the sensor to operate at low power stand-by mode. When a finger touches the sensing surface, an interrupt is generated. The interrupt signal can be used to wake up the processor which then turns on the sensing circuitry to capture fingerprint image.

#### 3.2 Reset

The hardware reset pin RSTN (active low) clears all the internal configuration, data buffer and state registers to the default values, and forces the chip to stay in idle mode.

When the hardware reset signal is removed, the chip remains in “software reset” mode until a 5-bit pattern 10110 (x16) is written to the RSTPAT register. The software reset can also be activated by issuing the SRST command (xC1) through the SPI interface.
The software reset command behaves the same way as the hardware reset, except the software reset does not clear the configuration registers that are set through the SPI register write command.

### 3.3 Power control

There are several control bits related to controlling the A-series power consumption:

- **EN4M (REG11[0])** - Enable/disable the main 4Mhz clock oscillator
- **EN6K (REG11[1])** - Enable/disable the low speed clock oscillator for finger detection
- **ENPWR (REG11[3])** - Enable/disable the analog voltage/current reference
- **ENADC (REG11[2])** - Enable/disable the analog core components

These control bits should be set properly according to the operation mode:

- In system idle or reset state, all the above control bits should be turned off
- For finger detection mode, the main functional modules can be turned off to save power, only the low speed clock oscillator should be turned on.
- For fingerprint capture operation, all the functional module should be turned on, except the low speed clock oscillator that can be turned off (although the low speed clock power is not a significant part of the total power consumption).

### 3.4 Finger detection mode and interrupt

The two IO pin T1 and T2 are multifunctional, which is described in section 4.3.

When ENDET (REG11[5]) is set, and all the power control bits are set correctly for the finger detection mode, the A-series chip stays in a low power stand-by mode, in which the chip wakes up periodically to sense finger touching the sensing area. The time period of sleep/wake-up is controlled by the 4-bit DETDIV (REG0[7:4]) and the 2-bit DETCLK (REG8[7:6]) registers:

- **DETCLK (REG8[7:6])** selects one of the 4 derived clock from the main 6Khz oscillator:
  - 0 selects 6Khz divided by 16 (or 625hz)
  - 1 selects 6Khz divided by 128 (or 78hz)
  - 2 selects 6Khz divided by 1024 (or 10hz)
  - 3 selects 6Khz divided by 8192 (or 1.2hz)
- **DETDIV (REG0[7:4])** then determines a divide factor which further divide the selected frequency by the 4bit value plus 1.
- So the wake-up frequency is can be calculated as following:

  \[
  \text{Detect\_Freq} = \begin{cases} 
  625, & \text{DETCLK} = 0 \\ 
  78, & \text{DETCLK} = 1 \\ 
  10, & \text{DETCLK} = 2 \\ 
  1.2, & \text{DETCLK} = 3 \\ 
  \end{cases} \times (\text{DETDIV}+1) 
  \]

The finger detection interrupt signal pin on T2 pin can be enabled by setting T2OE to 1 and setting
T2SEL (REG10[1:0]) to 10, which sends an active-high pulse to the processor when a finger touches the sensor. The sensitivity of finger detection can be adjusted by setting the 6-bit DETTH (REG8[5:0]) register. This value determines an internal threshold voltage. The higher value means it is less sensitive.

3.5 Data encryption

When data encryption is enabled, the image data is scrambled by a set of 8-byte keys and 12-bit rotation parameter stored in the OTP memory location 22~31, as illustrated below:

To enable OTP operation and load the stored keys and rotation parameters into the internal encryption engine, the firmware must send the 0x04 command. It is not necessary to use the 0x04 command between image frames, for the internal state of the encryption engine at the end of a image frame can be used as the initial state of the next frame as long as the firmware decoder keeps track of it.

In data encryption mode, there is a internally generated random data byte inserted at the beginning of each image frame. This means the first byte of the decoded image data should be ignored.

3.6 Sample sessions

Image capture

Assume all the analog settings remains as default, the following procedure summarizes the image capture and detection operation modes:

- Image capture procedure with encryption mode
  - hardware reset at power on
  - initialize OTP encryption table by writing the 0x04 command
  - write register 11:
    - turn on the 4Mhz oscillator by setting reg11[0] to 1
enable encryption mode by setting reg11[4] to 1
- turn on power and analog circuit by setting reg11[3:2] to 3
  o write the start_scan command (0x01)
  o read image data by the 0x02 command, the first captured image byte is random data and should be thrown away
  o during image transfer, firmware must check FIFO status by the status command 0x03.
  o alternatively, the FIFO status can be checked by probing the T2 port. This is done by setting T2OE (reg10 bit2) to 1 and T2SEL (reg10 bit[1:0]) to 01.

- Image capture procedure when encryption mode is off
  o hardware reset at power on
  o set normal operation mode and turn on oscillator by writing 0x0d to register 11.
  o write the start_scan command (0x01)
  o read image data by the 0x02 command
  o during image transfer, empty FIFO will return invalid code 0xFF. Code 0x00~0xFE are valid image data.

- Finger detection procedure
  o hardware reset at power on
  o turn on the 4Mhz oscillator by setting reg11[0] to 1
  o send the OTP initialization command 0x04 command
  o write 0x22 to register 11:
    - turn off analog power
    - turn off the 4Mhz
    - turn on the 6Khz clock
    - turn on detect mode
  o enable interrupt pin T2 by writing 110 to register 10, bit[2:0].
  o the T2 output polarity can be controlled by setting register 10, bit[3] -- 0 means active-high, and 1 means active-low.
  o wait for interrupt signal on pin T2

3.7 Timing considerations

The internal 4Mhz clock oscillator provides the time base for the logic design. The highest pixel sampling rate is half of it, i.e, 2Mhz. Using the 192x192 array as an example the entire image would roughly take 192x192x0.5 usec, or 19msec to capture the full frame image. This means a speed of more than 50 frames per second. However, there are timing delay at the start of scan, and between lines, so the real frame rate should be lower.

Optionally, the 4Mhz oscillator can be divided by a factor of 1~16, which is determined by the OSCDIV (REG0 bit [3:0]) control register. Setting OSCDIV to 0 gives the maximum speed and the value of 15 produces a clock of 4Mhz/16 = 0.25Mhz.
## 4.0 Additional features

### 4.1 Sub-scan mode

The image sub-scan or subsampling mode can be used to extract a smaller image by skipping 3 in every 4 column and rows. By setting register 11 bit 7, the smaller image can be captured like in the normal mode, but reduced to 1/16 of the original size.

### 4.2 OTP operation

Related control bits:

- Reg13, bit4~0: OTP address
- Reg14, bit7~0: OTP write data
- Reg15, bit7: PROG
- Reg15, bit6: NVSTR
- Reg15, bit1: AE
- Reg15, bit0: OE

Reading and Writing the OTP memory is performed by programming the OTP control bits according to the following timing chart:

<table>
<thead>
<tr>
<th>Read mode parameters</th>
<th>Symbols</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address setup time</td>
<td>Tas</td>
<td>2</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Address hold time</td>
<td>Tah</td>
<td>2</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>AE pulse high</td>
<td>Taerh</td>
<td>24</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>AE pulse low</td>
<td>Taerl</td>
<td>24</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>AE period time</td>
<td>Taer</td>
<td>48</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
4.3 Multifunction IO signals

The multifunction IO signal T1 and T2 are summarized in the following table:

<table>
<thead>
<tr>
<th>Write mode parameters</th>
<th>Symbols</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Address setup time</td>
<td>Tas</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Address hold time</td>
<td>Tah</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Data setup time</td>
<td>Tds</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Data hold time</td>
<td>Tdh</td>
<td>5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>NVSTR pulse high</td>
<td>Tnvhp</td>
<td>30</td>
<td>100</td>
<td>us</td>
</tr>
<tr>
<td>AE to NVSTR setup time</td>
<td>Taes</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>AE to NVSTR hold time</td>
<td>Taeh</td>
<td>3</td>
<td></td>
<td>us</td>
</tr>
<tr>
<td>AE pulse low</td>
<td>Taelp</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>PROG setup time</td>
<td>Tpgs</td>
<td>100</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>VPP to PROG setup time</td>
<td>Tvpps</td>
<td>1</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>VPP to PROG hold time</td>
<td>Tvpph</td>
<td>0</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>T1 pin</td>
<td>LTTEST = 0</td>
<td>T1SEL = 00</td>
<td>input</td>
<td>hardware reset</td>
</tr>
<tr>
<td>--------</td>
<td>------------</td>
<td>------------</td>
<td>-------</td>
<td>----------------</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T1SEL = 01</td>
<td>output</td>
<td>FIFO not empty</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T1SEL = 10</td>
<td>output</td>
<td>Detect Interrupt</td>
</tr>
<tr>
<td></td>
<td></td>
<td>T1SEL = 11</td>
<td>output</td>
<td>Active drive</td>
</tr>
<tr>
<td>LTTEST = 1</td>
<td></td>
<td>(reserved)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

| T2 pin | T2OE = 0     | T2SEL = 00 | input | (reserved) |
|        |              | T2SEL = 01 | input | (reserved) |
|        |              | T2SEL = 10 | input | external clock |
|        |              | T2SEL = 11 | input | chip enable | Active low |
|        | T2OE = 1     | T2SEL = 00 | output | (reserved) |
|        |              | T2SEL = 01 | output | FIFO not empty | Active high* |
|        |              | T2SEL = 10 | output | Detect Interrupt | Active high* |
|        |              | T2SEL = 11 | output | Active drive | Active low* |

* inverted by INVIO1 and INVIO2

According to the table above, the T1 pin is used as hardware reset input by default.

The T2 pin can be either input or output. When T2 is configured as external clock input, the internal 4Mhz oscillator is replaced by the external clock applied on T2. The SPISEL signal can be optionally gated by the T2 input pin when T2 is configured as a chip-enable signal. In this mode, SPISEL signal will take effect only when T2 pin is low.

Both T1 and T2 pin can be configured as output signal for one of the following: active drive, FIFO-not-empty status or finger detect interrupt.

When configured as output, the T1 and T2 signal polarity can be controlled by the INVIO1 and INVIO2 respectively.
Revision history

<table>
<thead>
<tr>
<th>Version</th>
<th>Purpose</th>
<th>Author</th>
<th>Approval</th>
</tr>
</thead>
<tbody>
<tr>
<td>V001-20181020</td>
<td>Initial release</td>
<td>ZPH</td>
<td>FCL</td>
</tr>
<tr>
<td>V002-20190515</td>
<td>1. Add suggestion for user flex cable on table 7.</td>
<td>HCL</td>
<td>FCL</td>
</tr>
<tr>
<td></td>
<td>2. Add Q-UV test and modify RCA information.</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>3. Update Mechanical Drawing.</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Contact information

ByNew Technologies Inc.
2F-1, No. 283, Sec. 2, Fuxing S. Rd.,
Da'an Dist., Taipei City 106, Taiwan (R.O.C.)
Tel: 886-2-27019770
e-mail: support@bynewonline.com