

# MBF110

## Solid-State Fingerprint Sensor

### Overview

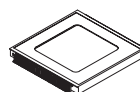
The Fujitsu MBF110 Solid-State Fingerprint Sensor is a direct contact, fingerprint acquisition device. It is a high performance, low power, low cost, capacitive sensor with an integrated two-dimensional array of metal electrodes in the sensing array. Each metal electrode acts as one plate of a capacitor and the contacting finger acts as the second plate. A passivation layer on the device surface forms the dielectric between these two plates. Ridges and valleys on the finger yield varying capacitor values across the array, which is read to form an image of the fingerprint.

The MBF110 is manufactured in standard CMOS technology and is available in an 80-pin, VSPA 80/1 and LQFP 80/1. The  $300 \times 300$  sensor array has a  $50 \mu\text{m}$  pitch and yields a 500-dpi image. The sensor surface is protected by a patented, ultra-hard, abrasion and chemical resistant coating.

### Features

- Non-optical solid-state device
- $300 \times 300$  sensor array,  $50 \mu\text{m}$  pitch
- $1.5 \text{ cm} \times 1.5 \text{ cm}$  sensor area
- 500-dpi resolution
- Operation from 3V to 5.5V
- Ultra-hard protective coating
- Integrated 8-bit flash analog-to-digital converter
- 8-bit microprocessor interface
- Standard CMOS technology
- Low power, less than 200 mW

### Packages



80-pin SOP (VSPA)



80-pin TSOP (LQFP)

A block diagram of the MBF110 is shown in Figure 1. The MBF110 has an integrated 8-bit flash analog-to-digital converter to digitize the output of the sensor array. The fingerprint image is transmitted on an 8-bit bi-directional bus interface compatible with most microprocessors.

For SETCUR resistor differences between the MBF110 see the Pin Information table.

### Applications

- Database and network access
- Portable fingerprint acquisition
- Access control (home, auto, office, etc.)
- ATM
- Smart cards
- Cellular phone security access



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Preliminary

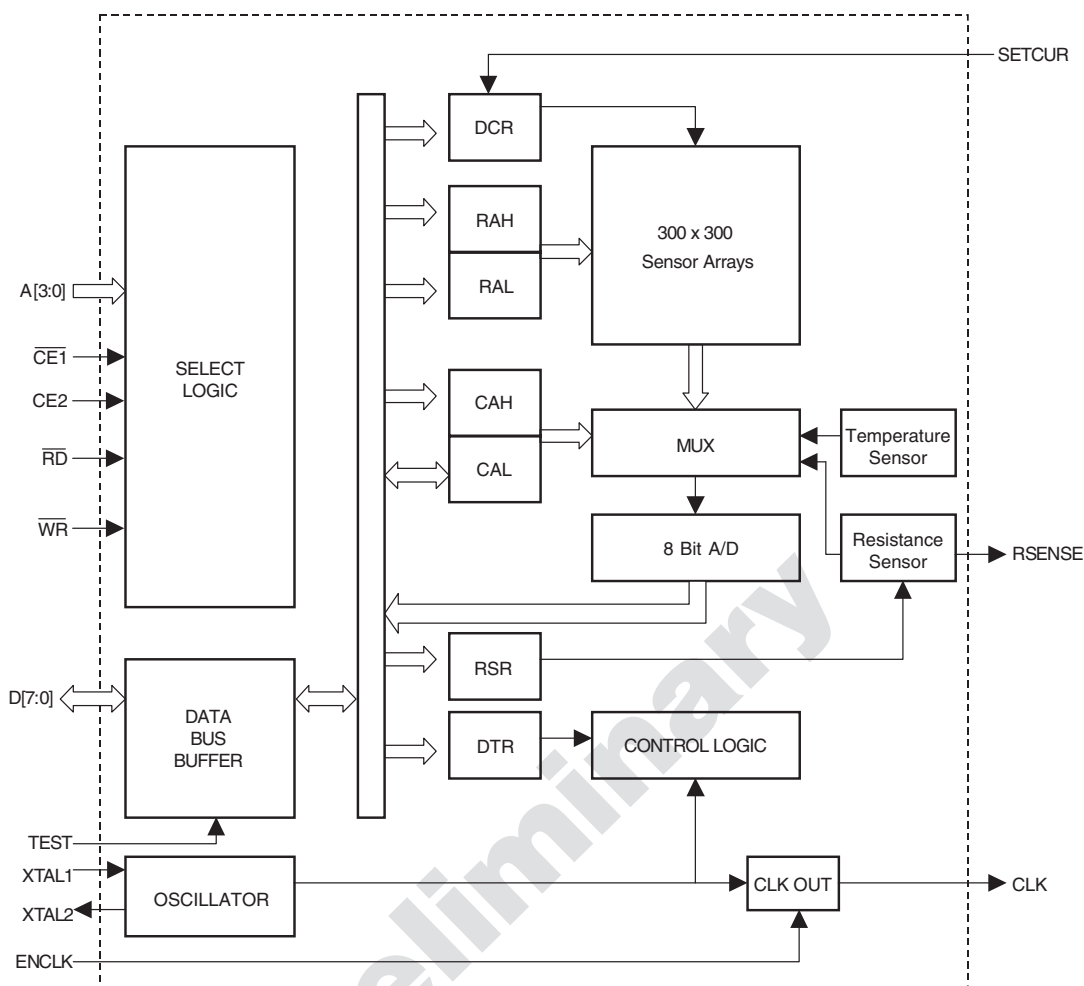


Figure 1. MBF110 Block Diagram

## Chip Operation

The sensor array is composed of 300 rows and 300 columns of sensor plates. Associated with each column are two sample-and-hold circuits. A fingerprint image is sensed or captured one row at a time. This “row capture” occurs in two phases. In the first phase, the sensor plates of the selected row are pre-charged to the  $V_{DD}$  voltage. During this pre-charge period, an internal signal enables the first set of sample-and-hold circuits to store the pre-charged plate voltages of the row.

In the second phase, the row of sensor plates is discharged with a current source. The rate at which a cell is discharged is proportional to the “discharge current.” After a period of time (referred to as the “discharge time”), an internal signal enables the second set of sample-and-hold circuits to store the final plate voltages. The difference between the pre-charged and discharged plate voltages is a

measure of the capacitance of a sensor cell. After the row capture, the cells within the row are ready to be digitized.

The sensitivity of the chip is adjusted by changing the discharge current and discharge time. The nominal value of the current source is controlled by an external resistor connected between the SETCUR pin and ground. The current source is controlled from the Discharge Current Register (DCR). The discharge time is controlled by the Discharge Time Register (DTR).

The sensor array is a row-oriented device. Images are read out one row at a time. The High-Order Row Address Register (RAH) and the Low-Order Row Address Register (RAL) must be programmed to select a row to be captured. Writing to RAL initiates a row capture. The capture time is a function of the external clock and the DTR. After the discharge cycle, the outputs of the row elements will be stored in analog sample and hold circuits.

# Solid-State Fingerprint Sensor

After the row capture is completed, the High-Order Column Address Register (CAH) and Low-Order Column Address Register (CAL) must be programmed to select an element within the captured row to be digitized. Writing to CAL causes the analog-to-digital (A/D) converter to digitize the difference between the outputs of the two sample-and-holds of the selected column cell. The output of the A/D converter is accessed by reading the CAL register.

Rows can be accessed in any order; however, the selected row must be captured before the column cells are read. The column cells within a row can be accessed in any order.

## Special Features

There are two programmable open-drain outputs that can be used for driving LEDs.

The CLKOUT pin can be enabled to output a square-wave clock of the same frequency as the oscillator clock. CLKOUT can be used to drive external circuitry. When ENCLK is high, the clock signal is present at the CLKOUT pin. When ENCLK is low or unconnected, the CLKOUT output is held low.

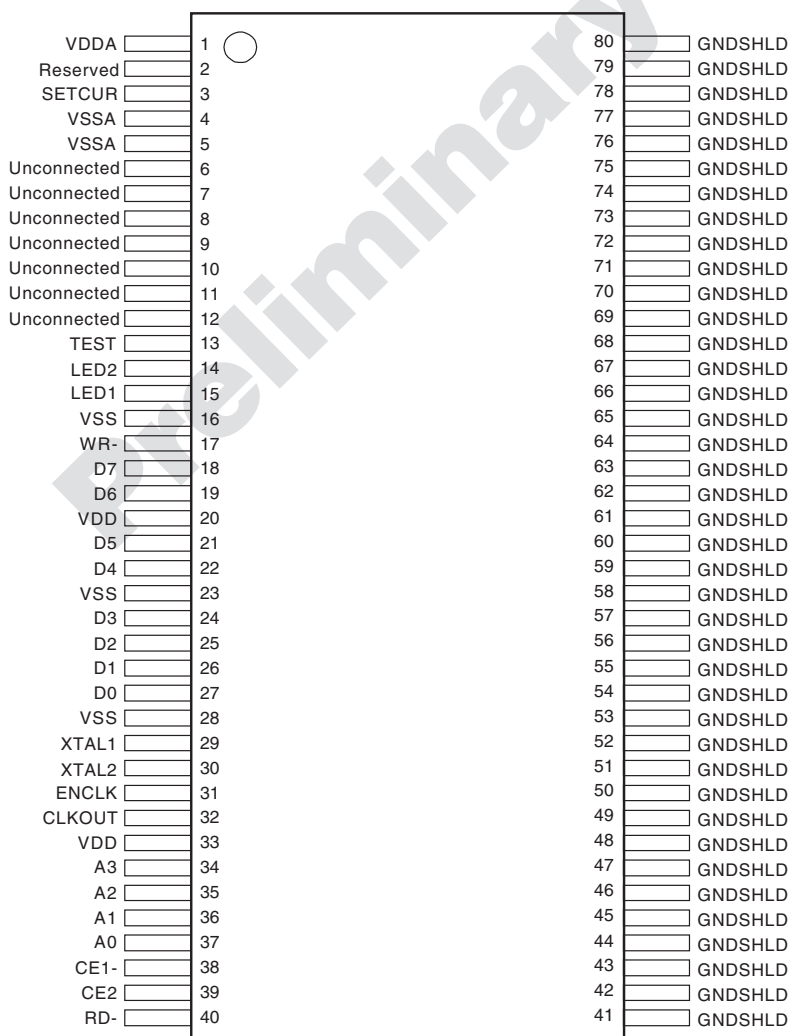
## MBF110 Pin Information for SOP (VSPA) 80/1

| Pin Number | Pin Name         | Type              | Description             | Notes  |   |
|------------|------------------|-------------------|-------------------------|--|---|
| 34         | A3               | Input             | Address Inputs          | Address signals connected to these pins select a register to read from or write to during data transfer.   |   |
| 35         | A2               |                   |                         |  |   |
| 36         | A1               |                   |                         |  |   |
| 37         | A0               |                   |                         |  |   |
| 38         | $\overline{CE1}$ |                   |                         |  |   |
| 39         | CE2              | Input             | Chip Enable, Active Low | When $\overline{CE1}$ is low and CE2 is high, the chip is selected.  |   |
| 39         | CE2              |                   |                         | Chip Enable, Active High   | When $\overline{CE1}$ is low and CE2 is high, the chip is selected.   |
| 40         | $\overline{RD}$  |                   |                         | Read Enable, Active Low  | This pin must be low while $\overline{WR}$ is high and the chip selected in order to read a register on the chip. |
| 17         | $\overline{WR}$  |                   |                         | Write Enable, Active Low   | This pin must be low while the chip is selected to write to a register on the chip.                               |
| 18         | D7               |                   |                         | Bi-directional   | Data Bus  |
| 19         | D6               |                   |                         |  |   |
| 21         | D5               |                   |                         |  |   |
| 22         | D4               |                   |                         |  |   |
| 24         | D3               |                   |                         |  |   |
| 25         | D2               |                   |                         |  |   |
| 26         | D1               |                   |                         |  |   |
| 27         | D0               |                   |                         |  |   |
| 32         | CLKOUT           | Output            | Clock Output            |  |   |
| 31         | ENCLK            | Input             | Enable Clock Output     | A high on this pin enables the CLKOUT pin. A low on this pin holds CLKOUT low. ENCLK has an internal pull-down resistor.                         |   |
| 15         | LED1             | Open-drain Output | LED driver              | This pin can be used to drive an LED.  |   |
| 14         | LED2             | Open-drain Output |                         |  |   |
| 3          | SETCUR           | Input             | Set Discharge Current   | Place an external resistor R1 (200K – 680K ohms) between this pin and ground. Typical: FPS110, R1 = 680K; FPS110B, R1 = 200K; FPS110E, R1 = 200K |   |
| 2          | N/A              |                   | Reserved pin            | Must be left disconnected.   |   |
| 13         | TEST             |                   |                         |  |   |
| 20, 33     | V <sub>DD</sub>  | Power             | Digital Power Supply    |  |   |
| 1          | V <sub>DDA</sub> |                   | Analog Power Supply     |  |   |

## MBF110 Pin Information for SOP (VSPA) 80/1 (Continued)

| Pin Number | Pin Name         | Type          | Description                      | Notes  |
|------------|------------------|---------------|----------------------------------|--|
| 16, 23, 28 | V <sub>SS</sub>  | Ground        | Digital ground                   |  |
| 4, 5       | V <sub>SSA</sub> | (Center)      | Analog ground                    |  |
| 29         | XTAL1            | Input         | Input to the On-Chip Oscillator  | To use the internal oscillator connect a crystal circuit to this pin. If an external oscillator is used, its output is connected to this pin. XTAL1 is the clock source for internal timing. |
| 30         | XTAL2            | Output        | Output of the On-Chip Oscillator | To use the internal oscillator connect a crystal circuit to this pin. If an external oscillator is used, leave XTAL2 unconnected.  |
| 41-80      | GNDSHLD          | Shield Ground | Connected to Package Top Plate   | These pins should connect to chassis ground.   |
| 2, 6-12    | N/A              | N/A           |                                  | Not connected.   |

## MBF110 Connection Diagram



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## Function Table

| $\overline{CE1}$ | CE2 | $\overline{RD}$ | $\overline{WR}$ | Mode        | Data Lines |
|------------------|-----|-----------------|-----------------|-------------|------------|
| H                | X   | X               | X               | De-selected | High-Z     |
| X                | L   | X               | X               | De-selected | High-Z     |
| L                | H   | H               | H               | Standby     | High-Z     |
| L                | H   | L               | H               | Read        | Data Out   |
| L                | H   | H               | L               | Write       | Data In    |

## Register Map

| A3 | A2 | A1 | A0 | Access     | Register | Description                        |
|----|----|----|----|------------|----------|------------------------------------|
| 0  | 0  | 0  | 0  | Write      | RAL      | Low Order Row Address Register     |
| 0  | 0  | 0  | 1  | Write      | RAH      | High Order Row Address Register    |
| 0  | 0  | 1  | 0  | Read/Write | CAL      | Low Order Column Address Register  |
| 0  | 0  | 1  | 1  | Write      | CAH      | High Order Column Address Register |
| 0  | 1  | 0  | 0  | Write      | DTR      | Discharge Time Register            |
| 0  | 1  | 0  | 1  | Write      | DCR      | Discharge Current Register         |
| 0  | 1  | 1  | 0  | Write      | RSR      | Reserved                           |

## Address Register Descriptions

Refer to *Row Capture and A/D Conversion Timing* on page 9 to calculate row capture and A/D conversion times.

### RAL (A3-A0 Address 0000) Write Only

### Low Order Row Address Register

This register and bit 0 of RAH form the 9-bit Row Address Register that selects the row to be captured. The 9-bit Row Address Register selects a row address from 0 through 299. Writing the RAL starts a row capture. Only RAL has to be written if RAH doesn't change, otherwise RAH has to be written before RAL.

| MSB  |      |      |      |      |      |      | LSB  |
|------|------|------|------|------|------|------|------|
| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
| RA7  | RA6  | RA5  | RA4  | RA3  | RA2  | RA1  | RA0  |

| Bit Number | Bit Name | Function                                |
|------------|----------|---|
| [7:0]      | RA[7:0]  | Low eight bits of Row Address Register. |



## RAH (A3-A0 Address 0001) Write Only

### High Order Row Address Register

Bit 0 of this register and RAL form the 9-bit Row Address Register that selects the row to be converted. The L1 and L2 bits control two open-drain outputs that can be used to drive LEDs.

| MSB  |      |      |      | LSB  |      |      |      |
|------|------|------|------|------|------|------|------|
| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
| L1   | L2   | –    | –    | –    | –    | –    | RA8  |

| Bit Number | Bit Name | Function  |
|------------|----------|---|
| 7          | L1       | L1=0, LED1 output low<br>L1=1, LED1 output high-Z   |
| 6          | L2       | L2=0, LED 2 output low<br>L2=1, LED 2 output high-Z |
| [5:1]      | –        | Reserved, write 0 to these bits.                    |
| 0          | RA8      | MSB of Row Address                                  |

## CAL (A3-A0 Address 0010) Read/Write

### Low Order Column Address Register

CAL is a read/write register. Writing to this address writes to the low-order 8 bits of the 9-bit Column Address Register. The 9-bit Column Address Register selects a column from 0 through 299. Writing to CAL causes the analog-to-digital (A/D) converter to

begin digitizing its input. The input of the A/D converter is selected by bits 7 and 6 of the CAH register. The user should wait until the row capture is completed before writing to the CAL.

Reading from this address returns the output of the A/D converter. After writing to CAL, the user should wait until A/D conversion completes before reading the A/D converter.

| MSB  |      |      |      | LSB  |      |      |      |
|------|------|------|------|------|------|------|------|
| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
| CA7  | CA6  | CA5  | CA4  | CA3  | CA2  | CA1  | CA0  |

| Bit Number | Bit Name | Function  |
|------------|----------|---|
| [7:0]      | CA[7:0]  | (WRITE) Low eight bits of Column Address Register.<br>(READ) Output of A/D converter. |

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## CAH (A3-A0 Address 0011) Write Only

### High Order Column Address Register

Bit 0 of this register and CAL form the 9-bit Column Address

Register that selects a cell from the current row for digitizing.

The user should wait until the row capture is completed before writing to CAH.

| MSB  |      |      |      |      |      |      | LSB  |
|------|------|------|------|------|------|------|------|
| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
| R    | T    | –    | –    | –    | –    | –    | CA8  |

| Bit Number | Bit Name | Function                         |
|------------|----------|----------------------------------|
| [7:1]      | –        | Reserved, write 0 to these bits. |
| 0          | CA8      | MSB of Column Address Register   |

## DTR (A3-A0 Address 0100) Write Only

### Discharge Time Register

| MSB  |      |      |      |      |      |      | LSB  |
|------|------|------|------|------|------|------|------|
| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
| PD   | T6   | T5   | T4   | T3   | T2   | T1   | T0   |

| Bit Number | Bit Name | Function  |
|------------|----------|---|
| 7          | PD       | Power down chip.<br>PD=0, Chip in Normal Mode<br>PD=1, Chip in Low Power Mode   |
| [6:0]      | T[6:0]   | Selects the count to be loaded into the Discharge Timer. Discharge time is selected in increments of the oscillator period. Discharge Time is defined as the period between the sampling and holding of the pre-charged sensor cell to the sampling and holding of the discharging sensor cell. The Discharge Time can be calculated from the following equation:<br><br>Discharge Time = T[6:0] * t <sub>osc</sub> |

## DCR (A3-A0 Address 0101) Write Only

### Discharge Current Register

| MSB  |      |      |      |      |      |      | LSB  |
|------|------|------|------|------|------|------|------|
| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
| F2   | F1   | TRST | DC4  | DC3  | DC2  | DC1  | DC0  |

| Bit Number | Bit Name | Function  |    |    |            |   |   |           |   |   |           |   |   |           |   |   |           |
|------------|----------|---|----|----|------------|---|---|-----------|---|---|-----------|---|---|-----------|---|---|-----------|
| [7:6]      | F2, F1   | <p>These two bits tell the chip the frequency of the external oscillator or crystal that is connected to the chip.</p> <table border="1"> <thead> <tr> <th>F2</th> <th>F1</th> <th>XTAL Input</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>10-15 MHz</td> </tr> <tr> <td>0</td> <td>1</td> <td>15-20 MHz</td> </tr> <tr> <td>1</td> <td>0</td> <td>20-30 MHz</td> </tr> <tr> <td>1</td> <td>1</td> <td>30-40 MHz</td> </tr> </tbody> </table> | F2 | F1 | XTAL Input | 0 | 0 | 10-15 MHz | 0 | 1 | 15-20 MHz | 1 | 0 | 20-30 MHz | 1 | 1 | 30-40 MHz |
| F2         | F1       | XTAL Input  |    |    |            |   |   |           |   |   |           |   |   |           |   |   |           |
| 0          | 0        | 10-15 MHz   |    |    |            |   |   |           |   |   |           |   |   |           |   |   |           |
| 0          | 1        | 15-20 MHz   |    |    |            |   |   |           |   |   |           |   |   |           |   |   |           |
| 1          | 0        | 20-30 MHz   |    |    |            |   |   |           |   |   |           |   |   |           |   |   |           |
| 1          | 1        | 30-40 MHz   |    |    |            |   |   |           |   |   |           |   |   |           |   |   |           |
| 5          | TRST     | <p>Timer Reset. Set this bit to halt and reset the Discharge Timer. Resetting the Discharge Timer is necessary to put the Discharge Timer in a known state after power-up or after returning to Normal mode from Low-power mode (See bit 7 of DTR).</p> <p>TRST=0, Normal Timer Operation<br/>TRST=1, Halt and Clear Discharge Timer (doesn't clear DTR)</p>  |    |    |            |   |   |           |   |   |           |   |   |           |   |   |           |
| [4:0]      | DC[4:0]  | Selects the Discharge Current source value.   |    |    |            |   |   |           |   |   |           |   |   |           |   |   |           |

## RSR (A3-A0 Address 0110) Write Only

### Reserved

The user must initialize this resistor to zero.

| MSB  |      |      |      |      |      |      | LSB  |
|------|------|------|------|------|------|------|------|
| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
| -    | -    | -    | -    | -    | -    | -    | -    |

| Bit Number | Bit Name | Function                         |
|------------|----------|----------------------------------|
| [7:0]      | -        | Reserved. Write 0 to these bits. |

# Solid-State Fingerprint Sensor

## Row Capture and A/D Conversion Timing

| F2 | F1 | XTAL Input Range | Row Capture Time in OSC Clock Periods | A/D Conversion Time in OSC Clock Periods |
|----|----|------------------|---------------------------------------|--|
| 0  | 0  | 10-15 MHz        | 18+n                                  | 13                                       |
| 0  | 1  | 15-20 MHz        | 24+n                                  | 15                                       |
| 1  | 0  | 20-30 MHz        | 36+n                                  | 23                                       |
| 1  | 1  | 30-40 MHz        | 48+n                                  | 30                                       |

NOTE: n is selected by bits T[6:0] of DTR.

## A/D Converter

The integrated 8-bit flash A/D converter is a buffered device. Each write to CAL causes: 1) the result of the previous conversion to be latched and made readable at CAL, and 2) the A/D converter to start digitizing its current input. Consequently, it takes 301 writes to CAL in order to digitize the 300 cells of a row.

## Specifications\*

\*All specifications in this document are preliminary and subject to change.

### Absolute Maximum Ratings

- Storage Temperature:  $-65^{\circ}$  to  $+150^{\circ}$  C
- DC Voltage Applied to any Pins:  $-0.5$  V to  $+7.0$  V

## Operating Range

| Symbol    | Parameter                  | Min              | Max  | Unit         |
|-----------|----------------------------|------------------|------|--------------|
| $V_{DD}$  | Digital Supply Voltage     | +3.0             | +5.5 | V            |
| $V_{DDA}$ | Analog Supply Voltage      | +3.0             | +5.5 | V            |
|           | Standard Temperature Range | 0                | 60   | $^{\circ}$ C |
| $f_{OSC}$ | Oscillator Frequency       | $V_{DD} = 5.0$ V | 40   | MHz          |
|           |                            | $V_{DD} = 3.0$ V | 20   | MHz          |

## DC Electrical Characteristics

| Symbol   | Parameter              | Test Conditions                    | Min  | Max      | Unit    |
|----------|------------------------|------------------------------------|------|----------|---------|
| $V_{OH}$ | Output High Voltage    | $V_{DD} = 4.5$ V, $I_{OH} = -4$ mA | 2.4  | –        | V       |
| $V_{OL}$ | Output Low Voltage     | $V_{DD} = 4.5$ V, $I_{OL} = 8$ mA  | –    | 0.4      | V       |
| $V_{OH}$ | Output High Voltage    | $V_{DD} = 3.0$ V, $I_{OH} = -2$ mA | 2.4  | –        | V       |
| $V_{OL}$ | Output Low Voltage     | $V_{DD} = 3.0$ V, $I_{OL} = 4$ mA  | –    | 0.4      | V       |
| $V_{IH}$ | Input High Voltage     |                                    | 2.0  | $V_{DD}$ | V       |
| $V_{IL}$ | Input Low Voltage      | $V_{DD} = 4.5$ V                   | -0.5 | 0.8      | V       |
| $V_{IL}$ | Input Low Voltage      | $V_{DD} = 3.0$ V                   | -0.5 | 0.6      | V       |
| $I_{LI}$ | Input Leakage Current  | $GND \leq V_{in} \leq 5.5$ V       | -5.0 | 5.0      | $\mu$ A |
| $I_{LO}$ | Output Leakage Current | $GND \leq V_{out} \leq 5.5$ V      | -5.0 | 5.0      | $\mu$ A |

## Power Supply Characteristics

( $V_{DD} = 5.5V$ ,  $f_{OSC} = 40$  MHz Standard Temperature Range)

| Symbol    | Parameter              | Test Conditions   | Typ |      | Max |      | Unit    |
|-----------|------------------------|---|-----|------|-----|------|---------|
|           |                        |   | LP  | STD  | LP  | STD  |         |
| $I_{DD1}$ | Digital Supply Current | Power down with CLKOUT disabled, (DTR bit 7 = 1, ENCLK = 0)               | <1  | 100  | 50  | 100  | $\mu A$ |
| $I_{DD2}$ |                        | Power down with CLKOUT enabled.<br>(DTR bit 7 = 1, ENCLK = 1)             | 17  | 20   | 20  | 25   | mA      |
| $I_{DD3}$ |                        | Idle with CLKOUT disabled.<br>(DTR bit 7 = 0, ENCLK = 0)                  | 8   | 10   | 12  | 15   | mA      |
| $I_{DD4}$ |                        | Idle with CLKOUT enabled.<br>(DTR bit 7 = 0, ENCLK = 1)                   | 17  | 20   | 20  | 25   | mA      |
| $I_{DD5}$ |                        | Active A/D conversion with CLKOUT disabled.<br>(DTR bit 7 = 0, ENCLK = 0) | 15  | 20   | 25  | 30   | mA      |
| $I_{DD6}$ |                        | Active A/D conversion with CLKOUT enabled.<br>(DTR bit 7 = 0, ENCLK = 1)  | 25  | 30   | 30  | 35   | mA      |
| $I_{DDA}$ | Analog Supply Current  | Power down with CLK disabled or enabled.<br>(DTR bit 7 = 1)               | <10 | <100 | 50  | 1000 | $\mu A$ |
|           |                        | IDLE with CLKOUT disabled or enabled,<br>(DTR bit 7 = 0)                  | 15  | 20   | 22  | 25   | mA      |
|           |                        | Active A/D conversion with CLKOUT disabled or enabled. (DTR bit 7 = 0)    | 18  | 22   | 26  | 30   | mA      |

Note: Analog supply currents are independent of  $f_{OSC}$

Note: XTAL2 & CLKOUT driving  $C_{LOAD} = 50pF$

## Power Supply Characteristics

$V_{DD} = 3.6V$ , Commercial Temperature Range,  $f_{OSC} = 20$  MHz

| Symbol    | Parameter              | Test Conditions   | Typ |     | Max |      | Unit    |
|-----------|------------------------|---|-----|-----|-----|------|---------|
|           |                        |   | LP  | STD | LP  | STD  |         |
| $I_{DD1}$ | Digital Supply Current | Power down with CLKOUT disabled.<br>( $V_{DD} = \max$ , $f_{OSC} = \max$ , DTR bit 7 = 1, ENCLK = 0)            | <1  | <10 | 50  | 100  | $\mu A$ |
| $I_{DD2}$ |                        | Power down with CLKOUT enabled.<br>( $V_{DD} = \max$ , $f_{OSC} = \max$ , DTR bit 7 = 1, ENCLK = 1)             | 6   | 10  | 10  | 15   | mA      |
| $I_{DD3}$ |                        | Idle with CLKOUT disabled.<br>( $V_{DD} = \max$ , $f_{OSC} = \max$ , DTR bit 7 = 0, ENCLK = 0)                  | 3   | 5   | 6   | 10   | mA      |
| $I_{DD4}$ |                        | Idle with CLKOUT enabled.<br>( $V_{DD} = \max$ , $f_{OSC} = \max$ , DTR bit 7 = 0, ENCLK = 1)                   | 6   | 10  | 10  | 15   | mA      |
| $I_{DD5}$ |                        | Active A/D conversion with CLKOUT disabled.<br>( $V_{DD} = \max$ , $f_{OSC} = \max$ , DTR bit 7 = 0, ENCLK = 0) | 6   | 10  | 10  | 15   | mA      |
| $I_{DD6}$ |                        | Active A/D conversion with CLKOUT enabled.<br>( $V_{DD} = \max$ , $f_{OSC} = \max$ , DTR bit 7 = 0, ENCLK = 1)  | 9   | 13  | 13  | 18   | mA      |
| $I_{DDA}$ | Analog Supply Current  | Power down with CLK disabled or enabled.<br>( $V_{DDA} = \max$ , DTR bit 7 = 1)                                 | <2  | <10 | 50  | 1000 | $\mu A$ |
|           |                        | IDLE with CLKOUT disabled or enabled, (DTR bit 7 = 0)   | 10  | 15  | 15  | 20   | mA      |
|           |                        | Active A/D conversion with CLKOUT disable or enable. (DTR bit 7 = 0)  | 12  | 15  | 18  | 25   | mA      |

Note: Analog supply currents are independent of  $f_{OSC}$

Note: XTAL2 & CLKOUT driving  $C_{LOAD} = 50$  Pf

# Solid-State Fingerprint Sensor

## Read Cycle Timing at $V_{DD} = 3.0V$ , Standard Temperature Range

| Parameter  | Description  | Min | Max | Unit |
|------------|--|-----|-----|------|
| $t_{AAC}$  | Address valid to data valid.                         | –   | 70  | ns   |
| $t_{RC}$   | Read Cycle Time                                      | 70  | –   | ns   |
| $t_{ACE1}$ | $\overline{CE1}$ low to data valid                   | –   | 70  | ns   |
| $t_{ACE2}$ | CE2 high to data valid                               | –   | 70  | ns   |
| $t_{DOE}$  | $\overline{RD}$ low to data valid                    | –   | 35  | ns   |
| $t_{LZOE}$ | $\overline{RD}$ low to low Z                         | 5   | –   | ns   |
| $t_{HZOE}$ | $\overline{RD}$ high to high Z                       | –   | 30  | ns   |
| $t_{LZCE}$ | $\overline{CE1}$ low and CE2 high to low Z           | 5   | –   | ns   |
| $t_{HZCE}$ | $\overline{CE1}$ high to high Z or CE2 low to high Z | –   | 30  | ns   |
| $t_{LZWE}$ | $\overline{WR}$ high to low Z                        | 5   | –   | ns   |
| $t_{HZWE}$ | $\overline{WR}$ low to high Z                        | –   | 30  | ns   |

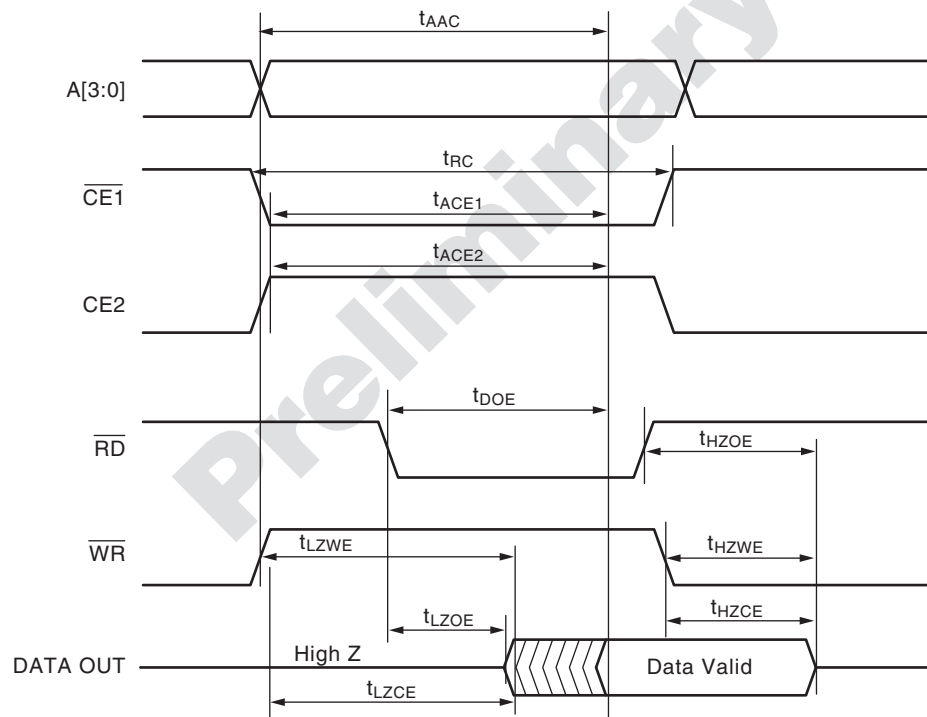


Figure 2. Read Cycle Timing

## Write Cycle Timing at $V_{DD} = 3.0V$ , Standard Temperature Range

| Parameter  | Description                       | Min | Max | Unit |
|------------|-----------------------------------|-----|-----|------|
| $t_{WC}$   | Write Cycle                       | 70  | –   | ns   |
| $t_{SCE1}$ | $\overline{CE1}$ low to write end | 60  | –   | ns   |
| $t_{SCE2}$ | CE2 high to write end             | 60  | –   | ns   |
| $t_{AW}$   | Address setup to write end        | 55  | –   | ns   |
| $t_{HA}$   | Address hold from write end       | 5   | –   | ns   |
| $t_{SA}$   | Address set-up to write start     | 5   | –   | ns   |
| $t_{PWE}$  | $\overline{WR}$ Pulse Width       | 40  | –   | ns   |
| $t_{SD}$   | Data setup to write end           | 35  | –   | ns   |
| $t_{HD}$   | Data hold from write end          | 5   | –   | ns   |

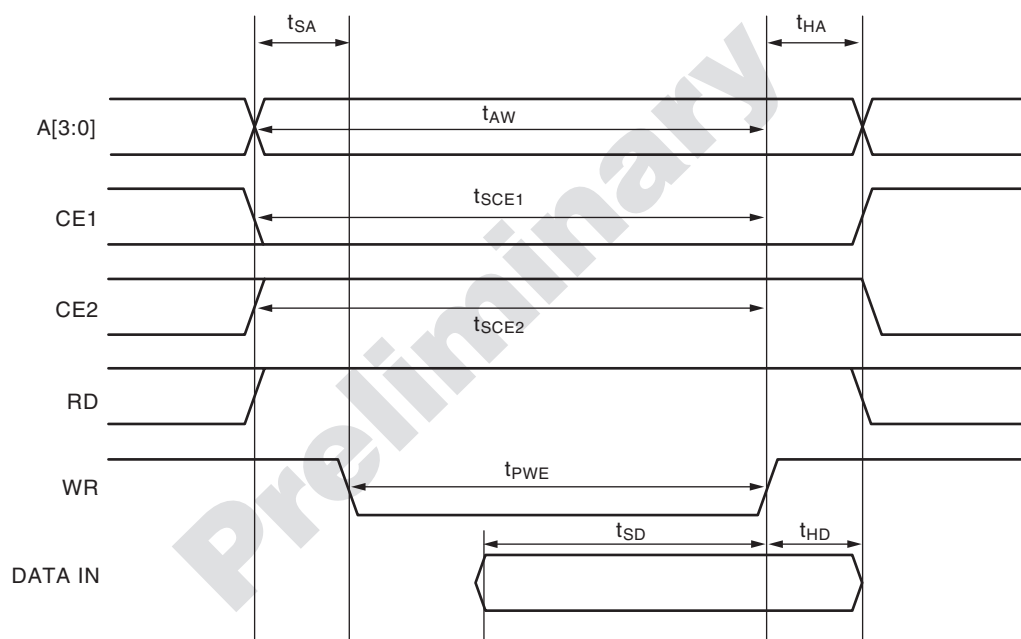
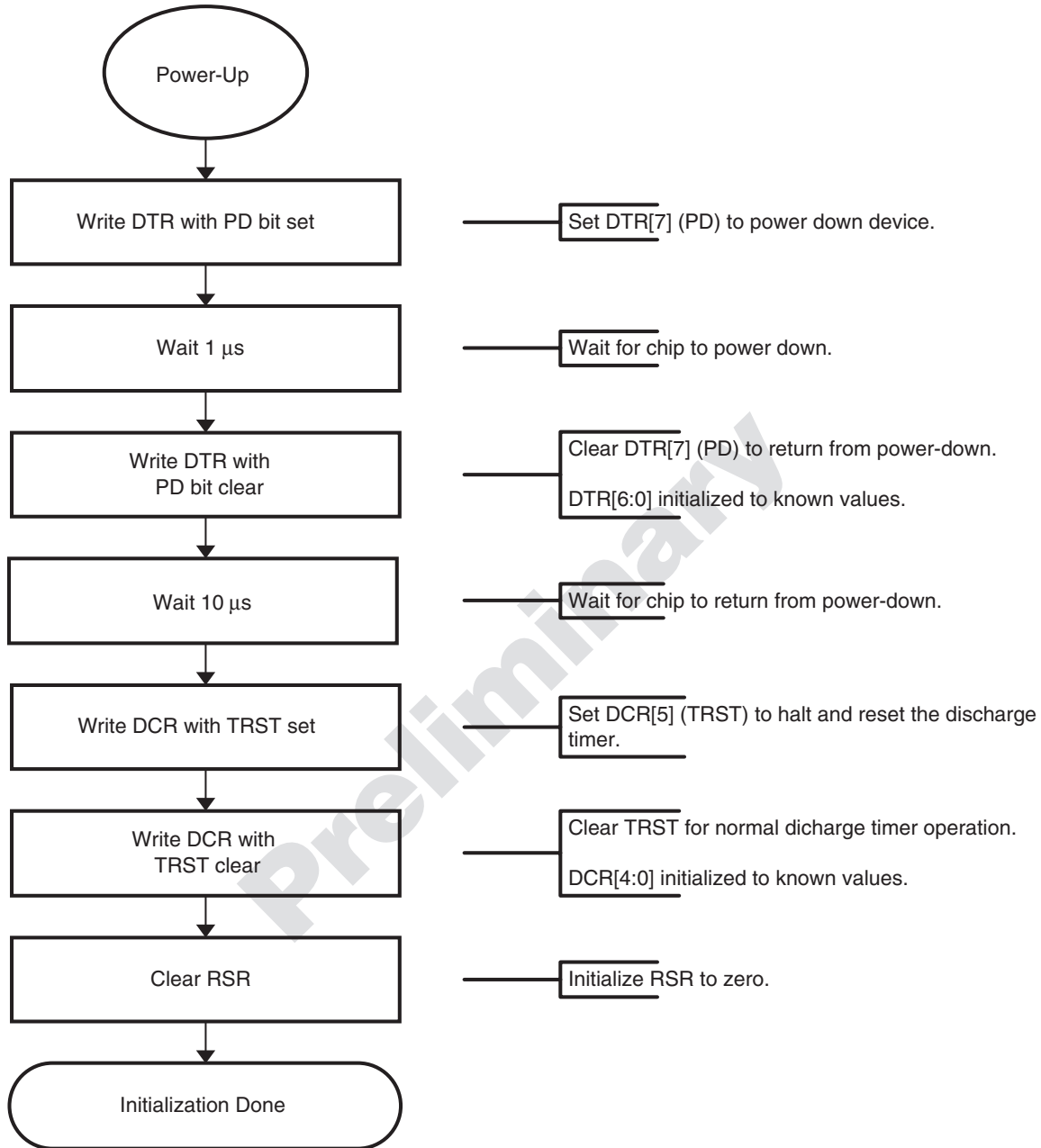


Figure 3. Write Cycle Timing

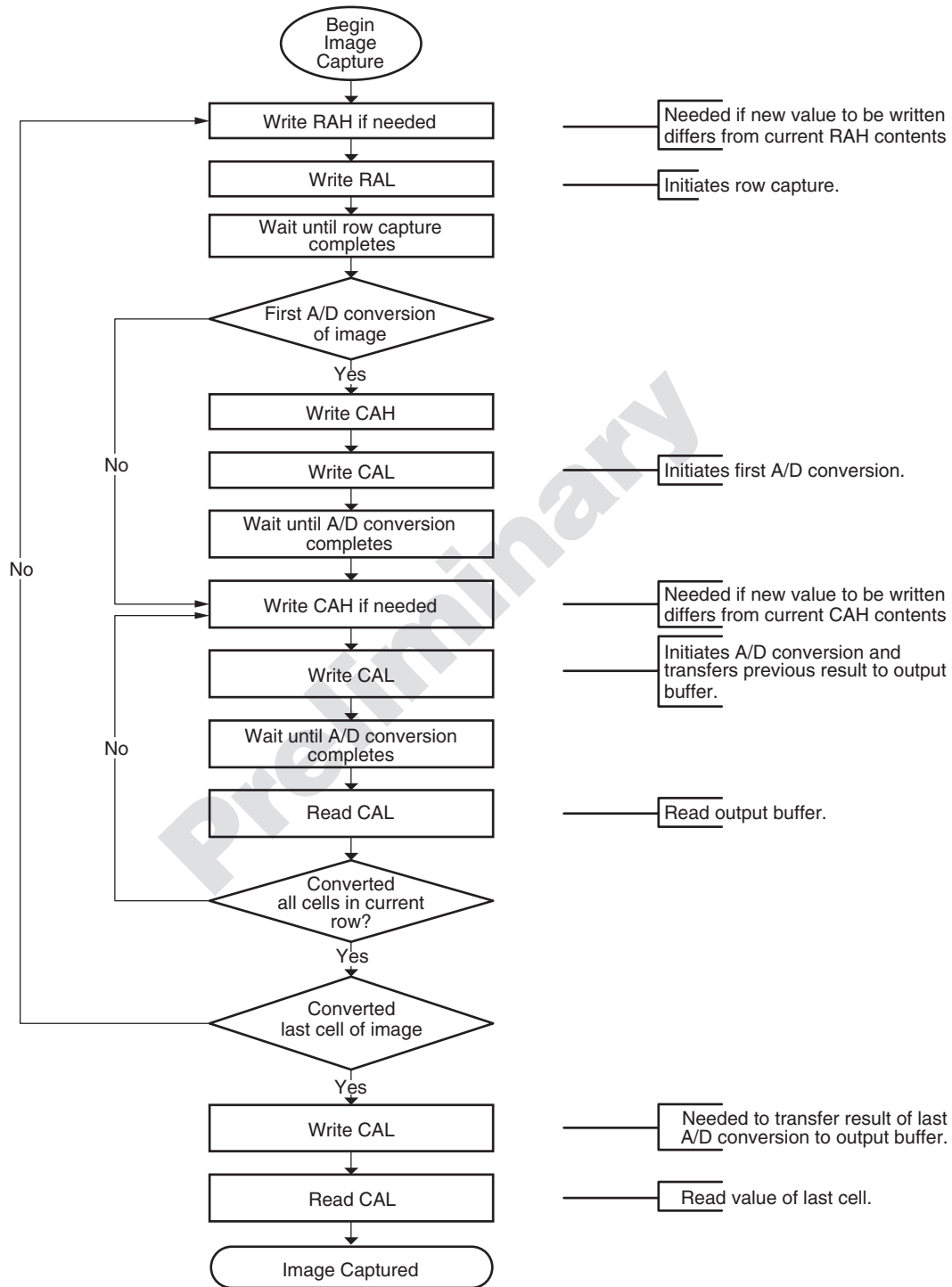
# Solid-State Fingerprint Sensor

## Power Up and Initialization





## Image Capture

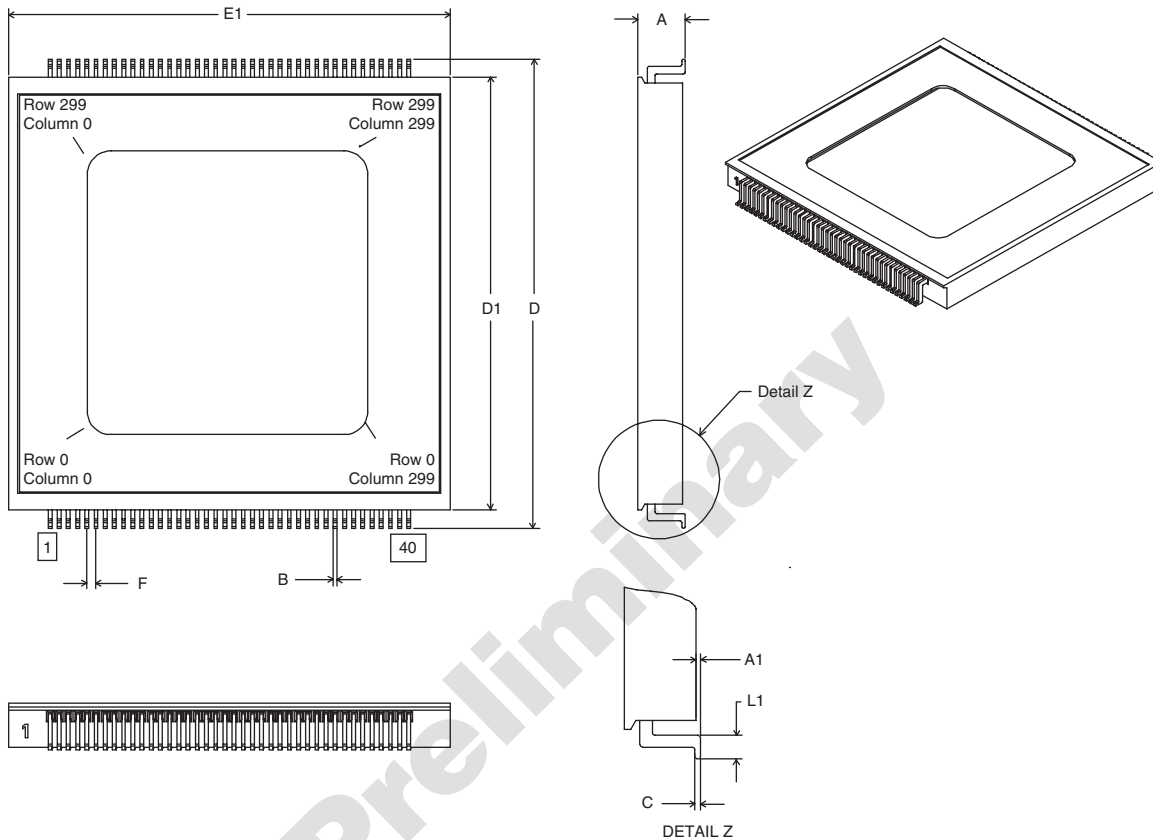


# Solid-State Fingerprint Sensor

## MBF110 – PFW1

### SOP (VSPA) – 80 pin Package

### MBF110-PFW1: SOP 80pin Assembly Diagram



MBF110 Dimensions

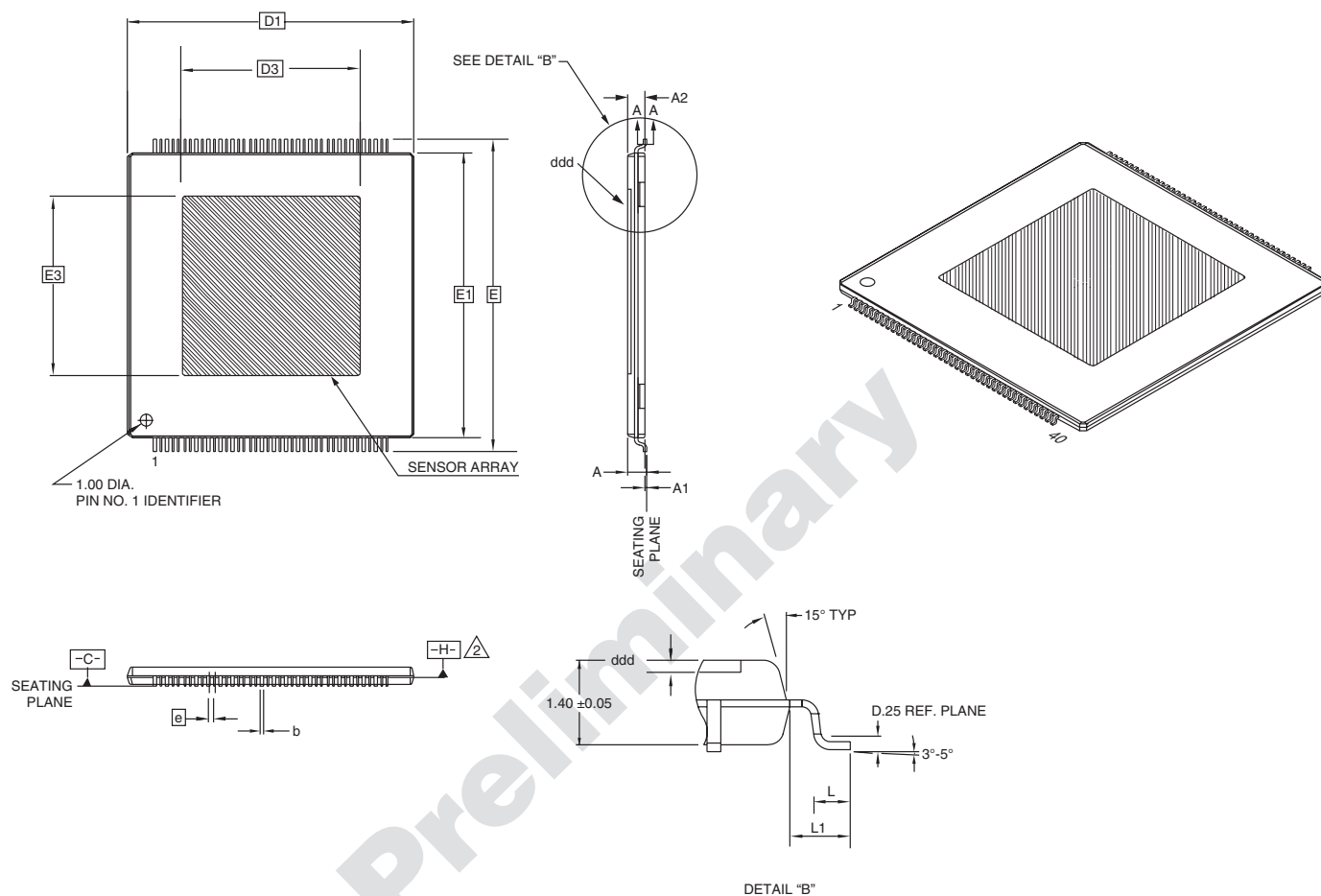
| Symbol | Description          | Min          | Nom          | Max          |
|--------|----------------------|--------------|--------------|--------------|
| N      | Pin Count            |              | 80           |              |
| A      | Overall Height       |              | .102 (2.60)  |              |
| A1     | Stand Off            |              | .006 (.15)   |              |
| B      | Pin Width            |              | .008 (.20)   |              |
| C      | Pin Thickness        |              | .008 (.20)   |              |
| D      | Tip to tip Dimension | 1.016 (25.8) | 1.025 (26.0) | 1.032 (26.2) |
| D1     | Package Body         | .941 (23.9)  | .945 (24.0)  | .949 (24.1)  |
| E1     | Package Body         | .941 (23.9)  | .945 (24.0)  | .949 (24.1)  |
| F      | Pin Pitch            | .0187 (.47)  | .0197 (.50)  | .0207 (.53)  |
| L1     | Foot length          |              | .032 (.81)   |              |

Note: Dimensions are in inches (mm)

## MBF110 – PFW

### TSOP (LQFP)– 80 pin Package

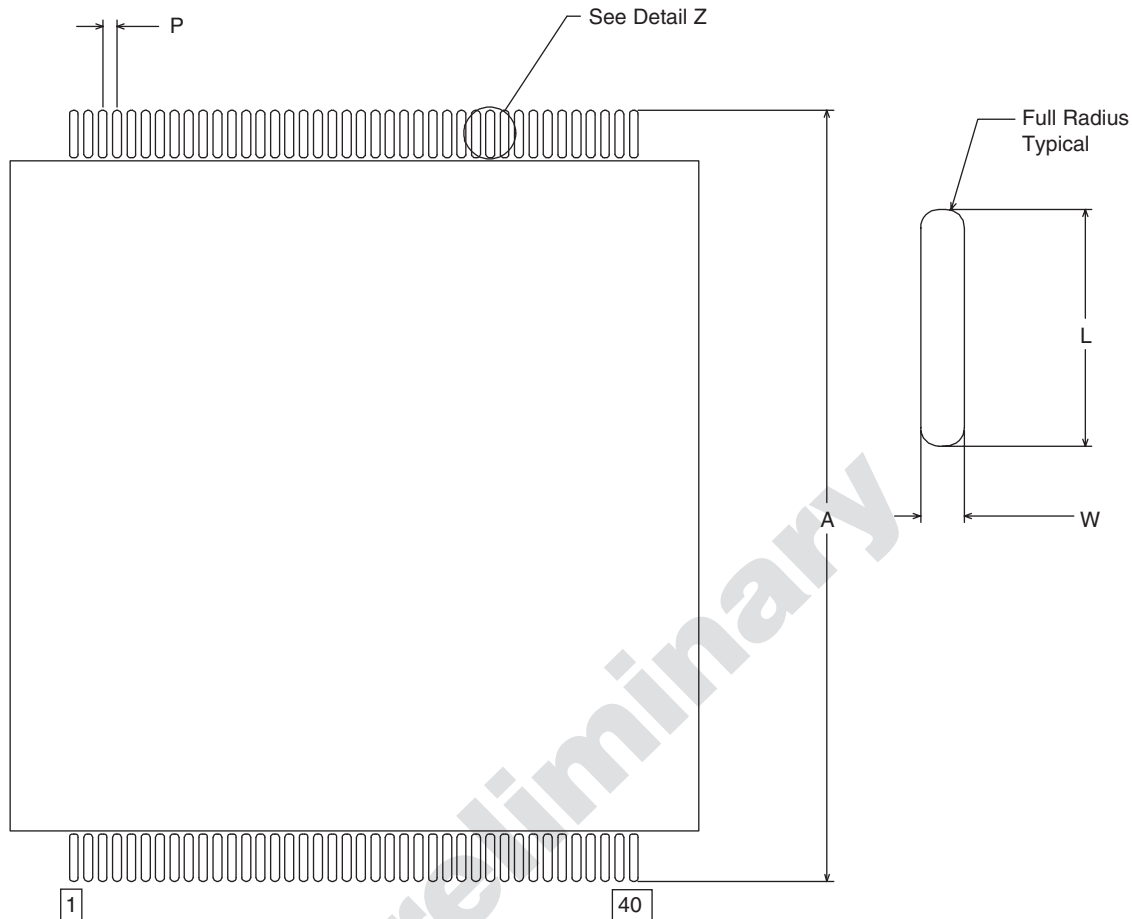
### MBF110-PFW: TSOP 80pin Assembly Diagram



| Symbol | Description          | DIMENSIONS  |            |       |        |            |      |
|--------|----------------------|-------------|------------|-------|--------|------------|------|
|        |                      | Millimeters |            |       | Inches |            |      |
|        |                      | Min.        | Nom.       | Max.  | Min.   | Nom.       | Max. |
| A      | Overall Height       | 1.45        | 1.55       | 1.70  | 0.57   | 0.61       | 0.67 |
| A1     | Stand Off            | 0.10        | 0.15       | 0.25  | .004   | .006       | .010 |
| A2     | Package Thickness    | 1.35        | 1.40       | 1.45  | .053   | .055       | .057 |
| b      | Lead Width           | 0.16        | 0.25       | 0.30  | .006   | .010       | .012 |
| D1     | Package Body         |             | 24.00 BSC. |       |        | .945 BSC.  |      |
| D3     | Sensor Array Width   | 14.95       | 15.00      | 15.05 | .588   | .590       | .592 |
| ddd    | Sensor Array Depth   | 0.25        | 0.30       | 0.35  | .010   | .012       | .014 |
| E      | Tip to Tip Dimension |             | 26.00 BSC. |       |        | 1.024 BSC. |      |
| E1     | Package Body         |             | 24.00 BSC. |       |        | .945 BSC.  |      |
| E3     | Sensor Array Height  | 14.95       | 15.00      | 15.05 | .588   | .590       | .592 |
| e      | Lead Pitch           |             | 0.50 TYP.  |       |        | .0197 TYP. |      |
| L      | Lead Length          | 0.50        | 0.60       | 0.70  | .020   | .024       | .028 |
| L1     | Foot Length          |             | 1.00 REF.  |       |        | .039 REF.  |      |

# Solid-State Fingerprint Sensor

## MBF110 Solder Pad Layout



| Symbol | Description          | Dimension     |
|--------|----------------------|---------------|
| N      | Pin Count            | 80            |
| A      | Tip to Tip Dimension | 1.074 (27.30) |
| P      | Pitch                | .0197 (.50)   |
| L      | Pad Length           | .065 (1.65)   |
| W      | Pad Width            | .012 (.30)    |

Note: Dimensions are in inches (mm)

## Manufacturing Considerations

**CAUTION: DO NOT USE ANY METAL PICKUP TOOLS WHICH WOULD CONTACT THE SENSOR DEVICE SURFACE WITHOUT PROTECTIVE LID INSTALLED**

- Surface Mount reflow temperature:
  - Recommended    220°C Max reflow spike\*
  - Max Temp        240°C
- Avoid any high pressure spray directly to the sensor device surface.
- Use standard handling practices for ESD sensitive devices.
- Refer to Fujitsu PCB Assembly for Biometric Sensor Guidelines.

## Array Pixel Specifications:

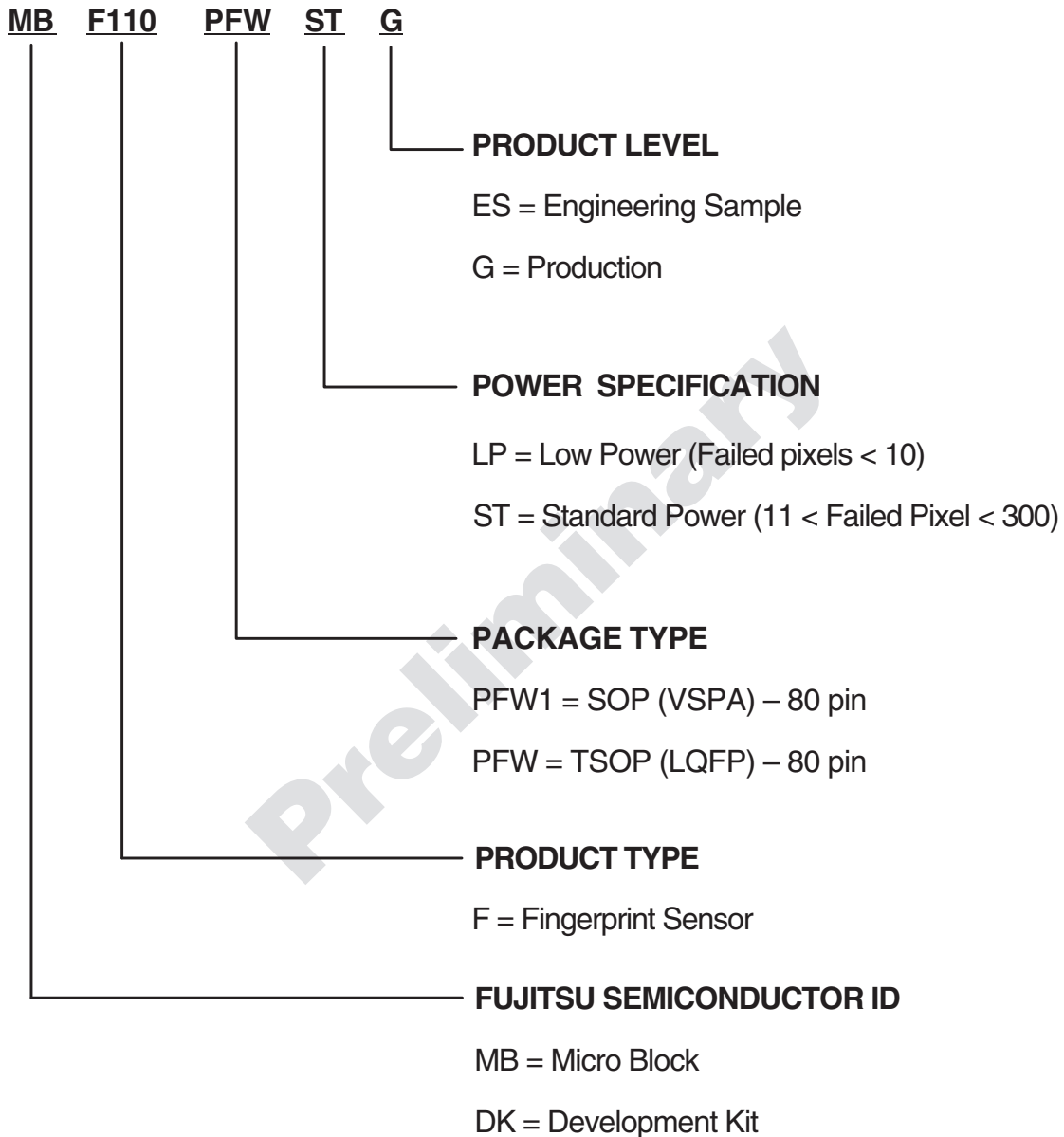
| Specification      | MBF110-LP | MBF110-STD     |
|--------------------|-----------|----------------|
| Max Failed Pixels  | 10        | 300            |
| Max Failed Rows    | 0         | 1 (see note 1) |
| Max Failed Columns | 0         | 1 (see note 1) |

Notes: 1) Failing rows or columns that fall on rows (0-4) or (295-299) or columns (0-4) or (295-299) are allowed to pass for the STD product due to packaging overlap at the edge of the sensor array. Failed rows or columns at the extreme edge of the array do not affect the quality of the acquired fingerprint image.

# Solid-State Fingerprint Sensor

## MBF110 Ordering Information

### MBF110 Part Number Description:





Preliminary

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