AuthenTec, Inc.

Personal Security for the Real World™

Product Specification

…for the AF-S2 Fingerprint Sensor

Hardware Reference

2087 Rev 1.3b
December 5, 2000

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Introduction

The *AF-S2 Product Specification* is a hardware reference manual. It provides detailed information on the functionality, operation, and interfaces of the FingerLoc™ AF-S2™ fingerprint image detection integrated circuit (IC). This device is developed and manufactured by AuthenTec, Inc.

The AF-S2 Sensor uses state-of-the-art techniques to capture and transmit a fingerprint from a user to a host computer. Reference Designs are available that can assist the developers in producing designs that take advantage of one of a number of well-known external communication protocols such as RS-232 asynchronous serial or the Universal Serial Bus (USB).

Note: This Product Specification may contain preliminary data. Users should be aware that information on AuthenTec's products, the Company, and other matters (including software updates) may be available on the AuthenTec web site at **www.authentec.com**.

For further information or guidance, contact AuthenTec's Application Engineering Department at **apps@authentec.com** for the latest product information.

Scope

The *AF-S2 Product Specification* is intended for the use of hardware designers, software designers, and others who require detailed information about the operation of the AF-S2 Sensor.

Applicability

This edition of the *AF-S2 Product Specification* is release version 1.3. It replaces all previous versions with changes that affect the technical data presented. Users should discard all previous editions of this document. The material in this document applies only to the AuthenTec AF-S2 Sensor IC.

Conventions

Vector Presentation

For vectors (groups of bits), ordering will always be from Most Significant Bit (MSB) to Least Significant Bit (LSB) (that is, Pixel_Data (Bit 47 – Bit 0) where bit 47 is the MSB and bit 0 is the LSB).

When vectors that span multiple bytes are transmitted, the lower byte (Bits 7 – Bit 0]) is transmitted first. This applies to pixel data and the Authentication Word that is returned after each imaging frame.

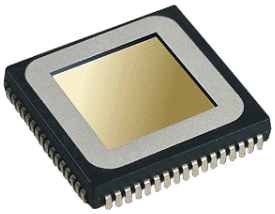
Typography

Numbers with the suffix “b” are presented in binary; numbers with an “h” are in hexadecimal.

Reference

This publication is prepared and presented in accordance with the guidelines and conventions of the *Microsoft Manual of Style for Technical Publications*, Microsoft Press, Redmond WA USA. Other reference material includes the *Chicago Manual of Style*, University of Chicago Press, Chicago IL, and the *IBM Dictionary of Computing*, Information Development, Poughkeepsie NY.

Overview



The AuthenTec **FingerLoc™ AF-S2™** integrated circuit fingerprint sensor is the second in a family of durable and extremely reliable semiconductor devices that can acquire a fingerprint image under the most rigorous real-world conditions.

The AF-S2 offers enhanced performance, improved flow control, and more user-selectable baud rates. It requires fewer supporting components, and so is more economical to implement than its predecessor, the AF-S1. It is completely plug-compatible with the earlier unit.

Hardware design considerations…

- Just drop in the AF-S2 in place of the AF-S1 - your hardware is upgraded!
- Save money by eliminating the rate converter from your current USB design.
- Save even more money with a minor layout change to reduce board size and assembly costs.

Software application considerations…

- A simple upgrade of the FingerLoc software is all that is required.
- New features of the AF-S2 sensor will be automatically used by familiar API calls in your current AS-S1 application.
- Operate legacy AF-SI systems at full functionality with the AF-S2 FingerLoc software.

Performance considerations…

- Faster image acquisition.
- Improved ability to acquire.
- Better recognition of “hard-to-get” fingers.

Product development considerations…

- Embedded controllers interface easily with the robust and flexible communication engine of the AF-S2.
- Reduced bandwidth allows more options in selecting the controlling processors.
- PC marketplace diversification is possible by lower cost solutions.

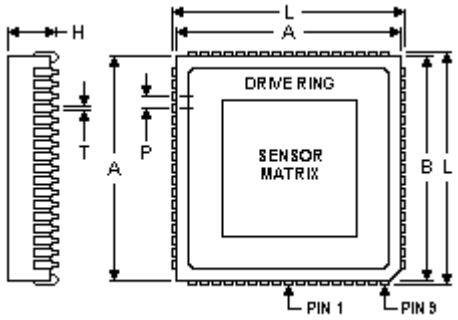
The AF-S2 is enabled and performance-enhanced by advanced imaging-control software – the **Dynamic Optimization**™ suite. This highly adaptive software mechanism automatically manages and performance-tunes the detection and acquisition process.

The native version of the AF-S2 Sensor supports standard RS-232 asynchronous serial communication and, with the addition of external components, the Universal Serial Bus.

Form Factor

The AF-S2 Sensor is packaged in a JEDEC-standard 68-pin PLCC (Plastic Leaded Chip Carrier) format. Physical dimensions (in millimeters) of this package are shown in the table below the illustration.

Figure: Sensor Dimensions



L		T		A		B		H	P
Min	Max	Min	Max	Min	Max	Min	Max	Max	Basic
25.02	25.27	0.33	0.53	24.13	24.33	24.13	24.33	3.50	1.27

Functional Summary of Operation

The sensorium of the AF-S2 is comprised of a sensor matrix, a drive ring, and supporting electronics. The purpose of these elements is to detect the presence of a finger placed on the surface of the sensor matrix, and to reliably produce a digital image of the fingerprint. This image must be suitable for processing through AuthenTec, AuthenTec Solution Provider, or third-party software for the purpose of identifying (authenticating) the person associated with the image.

The Sensor Matrix

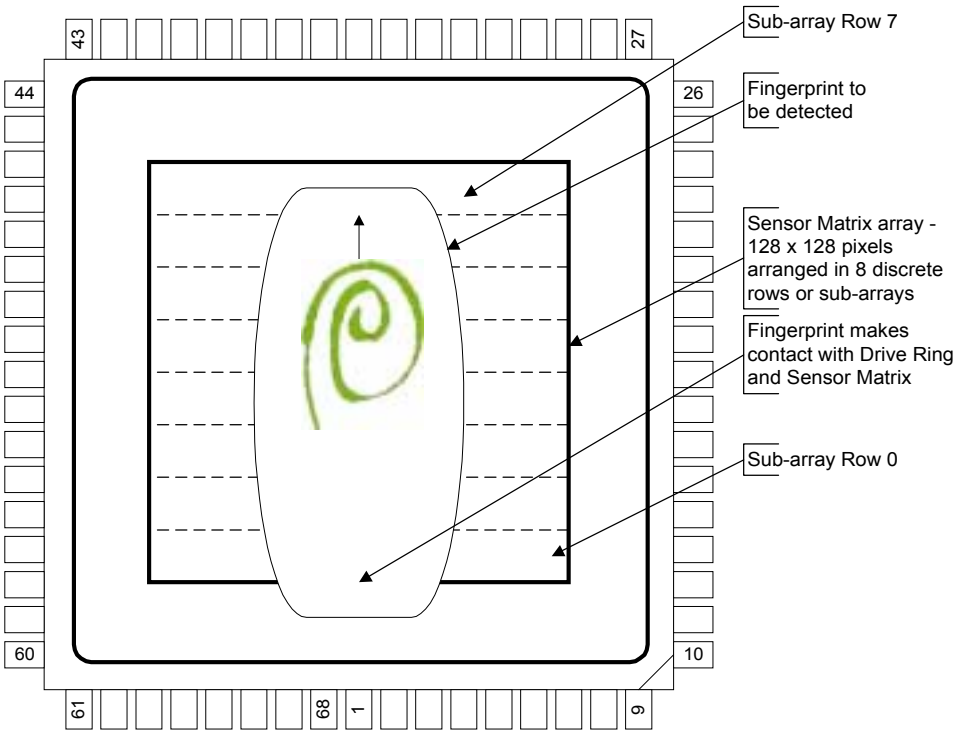
A fingerprint detection platen, the *sensor matrix*, occupies the center of the chip. This area is about 13mm (0.5 in) square, and is the actual surface of the integrated circuit die.

The surface of the *sensor matrix* is treated with a proprietary, advanced ceramic coating, having a Mohs hardness rating of 7+. The purpose of this layer is to protect the exposed IC and to generally resist abrasion and wear.

The *sensor matrix* is comprised of 16,384 individual elements arranged in a 128 x 128 square pattern. It is further organized into eight rectangular “sub-arrays” (numbered 0 through 7), each containing 128 columns of 16 pixels (2,048 elements). With the notched corner of the IC on the lower right (when viewed from the *sensor matrix* side) the sub-array rows are oriented in horizontal bands across the surface.

Each element in the *sensor matrix* is provided with an under-pixel amplifier, a synchronous demodulator, and a spatial filter node. Each sub-array row uses an on-chip multiplexer to combine the output of all 2,048 elements into a single set of 16 signals.

Figure: Sensor Matrix General Arrangement



The Drive Ring

The *sensor matrix* is surrounded by a three-millimeter-wide, rectangular, annular *drive ring*. The *drive ring* is the light-colored area seen in the preceding illustration.

The *drive ring* is excited by on-chip direct digital synthesis components that generate a sinusoidal signal. The phase, frequency, and amplitude of this signal are programmatically controlled through the use of the sensor control registers.

Operation

The *sensor matrix* is in effect an array of active antennas that receives the very small signal transmitted by the drive ring. The *drive ring* signal is coupled to and modulated by its passage through the subdermal structure of a finger that is placed on the image sensor (and also in contact with the drive ring, see preceding illustration) to create a pattern that accurately mimics the configuration of this living layer of skin.

A fingerprint image is scanned by digitizing the outputs from one sensor row at a time in a programmed sequence. The default is from Row 2 through Row 1, wrapping back from Row 7 to Row 0, starting at the rightmost column. The AF-S2 offers the capability of starting and stopping the scan at a user-selectable sub-array.

This permits the programmer to establish a strategy for which portion of the fingerprint is to be scanned. A shorter scan period can result in quicker settling of Automatic Gain Control (AGC) software and a thus a consequent saving in real time.

During imaging, power is applied to a given column in a selected row, enabling the selected column to drive an analog channel bus. The analog channel is amplified, integrated, and presented to *sample* and *hold* circuits. The sample and hold outputs are digitized and are then available as an asynchronous serial data stream.

Functional Features

The following is a high-level feature list for the AF-S2:

- Programmable finger-on detection rate. The AF-S2 remains in *Idle* mode between the 128µs detection periods (Register 8Ah).
- Independent control of stimulus frequency and amplitude for *Detect* and *Measure* modes (Registers 8Bh and 98h).
- Settable settling delay period to minimize transition to *Measure* mode due to noise (Register 8Dh).
- Automatic transition to *Measure* mode after detecting a finger. This feature can be over-ridden so that the AF-S2 remains permanently in *Measure* mode (Register 90h).
- Adjustable bias for the under-pixel amplifiers (Register 90h).
- Float or ground the inputs to unused under-pixel amplifiers (Register 90h).
- Adjustable phase of the demodulation signal relative to the stimulus (Register 8Ch).
- Settable column scan period. (Register 8Fh)
- Settable horizontal and vertical size of the high-pass spatial filter, or disable it (Register 92h).
- Adjustable analog channel bias (Register 8Fh) and gain (Register 91h).
- Adjustable low (Register 8Eh) and high (Register 8Dh) reference voltages for the D/A converter, thus increasing the effective dynamic range of the sensor's three-bit converter.

- Programmable Challenge Word for data authentication. The Challenge Word is used along with an embedded word and the pixel data to generate an Authentication Word. The Authentication Word is used to verify that the pixel data is valid information from an AF-S2 sensor (Registers 82h – 86h).

Users of the previous version of the sensor will find that the following additional features are new with the AF-S2:

- On-chip histogramming of the whole array, or just on the center 64 x 64 pixels (Register 80h).
- Programmable control over the start and end sub-array row used for imaging. (Register 89h).
- Adjustable column scan duty cycle to maximize the time available for A/D signal integration (Register 81h).
- Image scan process can be paused to compensate when the host is unable to accept data. (Register 80h).
- Alternate data representations (Register 8Ah)…
  - Two three-bit pixels per byte.
  - Eight three-bit pixels per three bytes.
  - Six one-bit pixels per byte.
  - Eight one-bit pixels per byte.

Component Description

The following block diagram shows a high-level view of the AF-S2 interface groups. The table below provides brief descriptions of each of these interfaces.

Figure: Sensor Interface Block Diagram

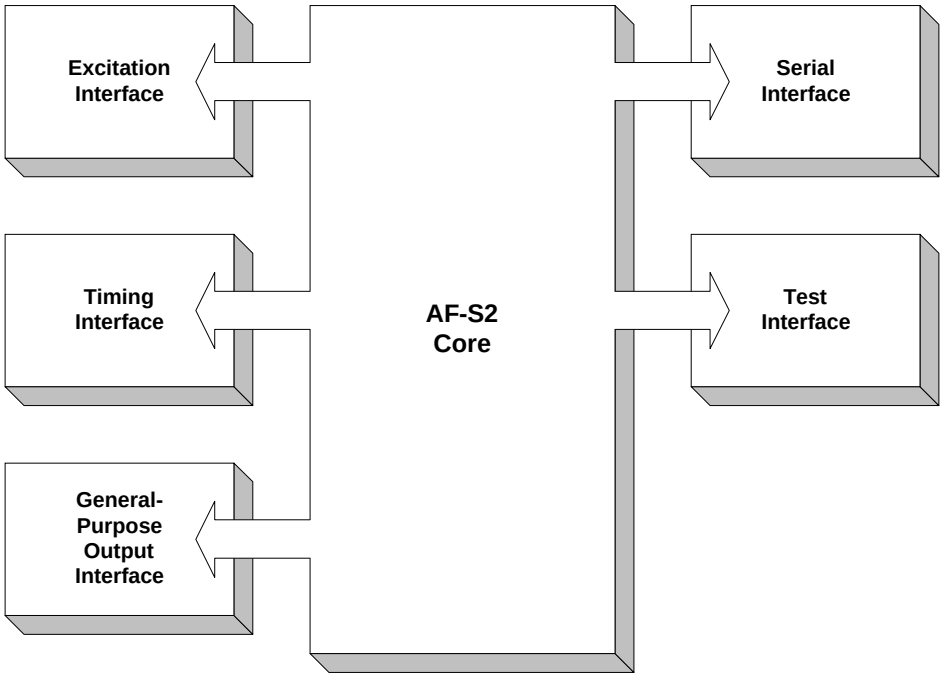


Table: Sensor Interface Descriptions

INTERFACE	DESCRIPTION
Serial Interface	This interface provides serial control and serial response for the AF-S2, including pixel data and current register settings. The data rate and format of the serial link are selectable. A detailed description of the serial interface is found in the following section.
Test Interface	This interface provides additional control and visibility for testing of the analog elements of the AF-S2.
Timing Interface	This interface provides clock and reset signals. Additional information on this interface is found in the following section.
Excitation Interface	This interface provides low level control and array power for image extraction. Additional information on this interface is found in the following section.
General-Purpose Output Interface	This interface provides a facility to control external devices such as LEDs or relays. Each output can source up to 5ma. The interface can be set to flash at various rates.

Serial Interface

The AF-S2 uses eight-bit data, one start bit, one stop bit, and no parity.

Communication follows one of four specific protocols. Command bytes are followed by one or more data bytes, described in the section Image Data Formats.

The following table lists the AF-S2 command-byte definitions.

Table: Command-Byte DefinitionS

COMMAND BYTE	DEFINITION
80h – 9Fh	Precedes a one-byte AF-S2 register data byte.
A0h - BFh	Reserved.
C0h – C7h	Precedes the 344-pixel data message formatted as six one-bit pixels per byte. The lower three bits indicate the sub-array row.
C8h - CFh	Reserved
D0h – D7h	Precedes the 258-pixel data message formatted as eight one-bit pixels per byte. The lower three bits indicate the sub-array row.
D8h - DDh	Reserved
DEh	Precedes the 16-byte histogram message.

COMMAND BYTE	DEFINITION
DFh	Precedes the eight-byte Authentication Word
E0h – E7h	Precedes 1,024-pixel data message for sub-array #0 through 7, respectively, formatted as two three-bit pixels per byte
E8h –EFh	Reserved
F0h –F7h	Precedes 768-byte pixel data message formatted as eight three-bit pixels per three bytes. The lower three bits indicate the sub-array row.
F8h –FFh	Reserved

Register Data Format

When a request to read registers is received, initiated by a rising edge on the *Read Registers* bit (Bit 1 in the BIT Control Register, Register 81h), all 32 register values are returned, each preceded by the command byte for the register, yielding a total of 64 bytes.

The command byte for the first register (80h) is sent first, followed by its data byte. This is followed by the command byte for the second register (81h) and its data byte and so on until finally the last register command (Register 9Fh) is sent, followed by the byte that defines the contents of that register.

Image Data Formats

While in *Measure* mode, pixel data for each of the eight sub-arrays is returned as it is received. Data for each sub-array is preceded by the command byte for that sub-array as seen in the preceding table, Command-Byte Definitions. The AF-S2 scans by default from the bottom up (the Pin 1 edge) and from the right to the left, unless otherwise specified by Register 89h.

> **Note:** When using AuthenTec's API, all image data formats described in this section are converted to standard eight-bit format.

Several alternate image data representations can be specified by the *Data Format* bits in Register 8Ah. Here are these representations in descending order of required bandwidth:

- **Two three-bit pixels per byte** – A three-bit pixel has eight levels of gray scale, in which level zero indicates "no ridge", up to level seven, indicating "ridge"), arranged in the byte as 0AAA0BBB. This default data representation yields 1,024 bytes of data per sub-array scan.
- **Eight three-bit pixels per three bytes** – A three-bit pixel has eight levels of gray scale, in which level zero indicates "no ridge", up to seven, indicating "ridge"), arranged as AAABBBCC CDDDEEEF FFGGGHHH.

This data representation yields 768 bytes of data per sub-array scan.

- **Six one-bit pixels per byte** – A one-bit pixel gives a binary representation of the fingerprint image data, in which 0 indicates “no ridge” and 1 indicates “ridge”, arranged as 0ABC0DEF. This data representation yields 344 bytes of data from the scan of each sub-array. The last two bytes and the last six pixels of the third-to-last byte are padded with zeroes.

- **Eight one-bit pixels per byte** – A one-bit pixel gives a binary representation of the fingerprint image data, in which 0 indicates “no ridge” and 1 indicates “ridge”, arranged as ABCDEFGH. This data representation yields 258 bytes of data per sub-array scan. The last two bytes of the row are padded with zeroes.

Description of a Typical Scan

When a default scan begins, the first byte received is the command byte (E0h). This is the header for the first sub-array of the scan, and is followed by 1,024 data bytes. The first data byte contains in its lower nybble (the AAA in the above example) the data for the first pixel (the lowermost pixel (row #0) in the rightmost column (column #0)). Its upper nybble (the BBB in the above example) contains the data for the second pixel (the next higher pixel (row #1, column #0)).

Each sub-array column is made up of eight data bytes for a total of 16 pixels. After the eight data bytes for column #0 is sent, the eight data bytes for column #1 is sent, and so on until the entire sub-array (through column #127) has been sent. Then, the next sub-array command header (E1h) is received, followed by its 1,024 data bytes, and so on.

After all data for all eight sub-arrays is sent, the authentication message is sent, preceded by the command byte for the Authentication Word (DFh). The eight-byte Authentication Word is sent low-order byte first.

The 32 register values are then returned, with each register preceded by the command byte for that register.

Test Interface

This interface provides additional control and visibility for testing of the analog and digital elements of the AF-S2. Digital features can be tested using boundary scanning techniques. The test interface is for the use of AuthenTec personnel only.

Timing Interface

An internal Phase Lock Loop (PLL) circuit generates an internal 32Mhz clock signal from an external 16Mhz crystal.

Excitation Interface

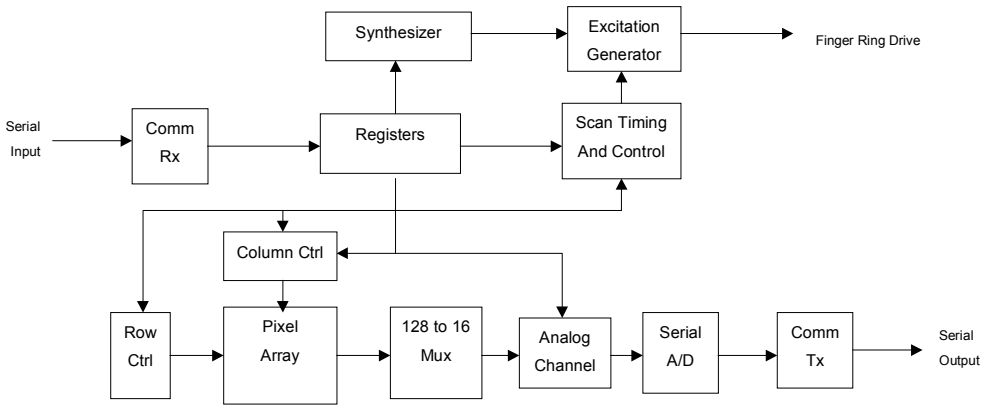
The Excitation Interface powers the finger excitation structure. The conductive Drive Ring located around the periphery of the sensor matrix may be used directly, or in conjunction with a conductive finger guide.

General-Purpose Output Interface

This interface provides a facility to control external devices such as LEDs or relays. Each output can source up to 5ma. The interface can be set to flash at various rates.

Operational Description

Figure: AF-S2 Functional Block Diagram



Control data is written asynchronously to a buffer. Prior to an image scan, before a detection cycle, or when triggered by an *Ops Reset* (Register 80h), the data in the buffers is written into registers.

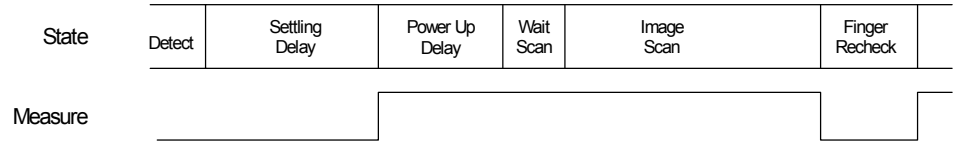
The AF-S2 is in *Idle* mode after a reset. In this mode, array power is turned OFF, and the sensor checks for a finger present at a rate programmed by the *Finger Detect Rate* setting (Register 8A). The reset value for this field puts the sensor into continuous *Detect* mode, where the internal excitation generator is always ON (at a frequency and amplitude determined by the *Detect Frequency* (Register 98h) and *Detect Drive* (Register 8Bh) settings). Other settings result in the excitation generator being turned ON for 128µs at the programmed rate.

A synchronous phase detector is used to compare the phase of the signal at the finger drive output (FDRV) with an internal reference signal. The internal reference is the excitation generator output with a delay determined by the *Res* (Register 9A) and *Cap* (Register 99) settings. The phase detector output is used to indicate if a finger is present. It is active when the finger drive signal is delayed by more than the reference signal.

The following timing diagram shows the sensor states related to when *Measure* mode is active. A programmable delay period (set by the *Finger Settling Delay* bits in Register 8D) begins when the finger detection output stays active. The

delay period is restarted if the finger detection output goes inactive.

Figure: Sensor States



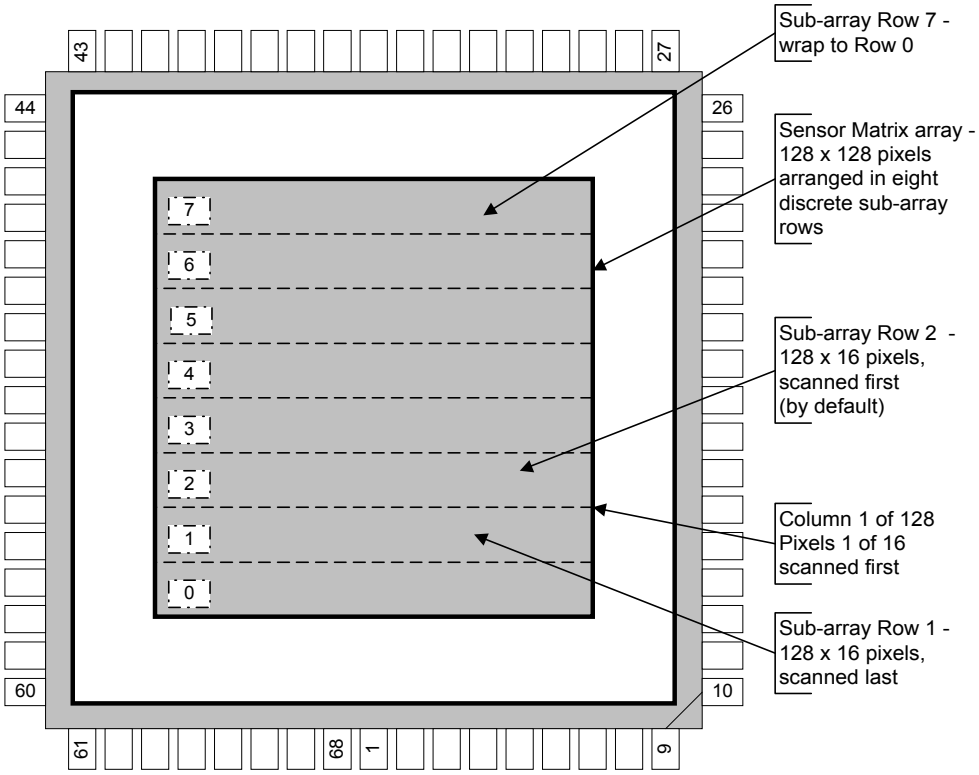
After the *Finger Settling Delay* time period has elapsed with the finger detection output HIGH, the array power is turned ON and the AF-S2 switches to *Measure* mode. In this mode, the frequency and amplitude of the excitation generator are determined by the *Measure Frequency* (Register 8Bh) and *Measure Drive* (Register 8Fh) settings. Also, the finger detection output is considered not valid in *Measure* mode (since the *Detect* and *Measure* frequencies can be different) and is not used. A fixed power-up delay of 32.768ms occurs before imaging begins.

Before beginning an image scan, the AF-S2 waits for certain conditions to be met:

- The serial port is not sending data
- *TxEnable* is asserted (the host is ready to receive data)
- Scanning is enabled (either via the continuous scan bit or a single trigger).

When these conditions are met, local registers are updated from their buffers and image scanning begins.

Figure: Sub-Array Row Numbering



The array layout and row numbering are shown in the preceding illustration. Each row consists of 128 columns of sixteen pixels, so the complete array comprises 128 rows x 128 columns.

Unless otherwise specified (Register 89h), Sub-array 2 is scanned first, followed by Sub-array 3, and so on in ascending numerical order. When the scan of Sub-array 7 is complete, the focus of attention wraps to Sub-array 0, finally completing the process at the end of Sub-array 1.

During imaging, Column 1 in a sub-array is scanned first, starting with Pixel 1(this pixel is in the bottom right corner of the sub-array, as shown in the preceding illustration). This column is powered up and the signals from each of the under-pixel amplifiers are demodulated, sampled, digitized, and sent to the host computer. Adjacent columns are also powered up in accordance with the *Z-Matrix Horizontal Pattern* setting (Register 92h), and pixels in adjacent rows are also powered using the *Z-Matrix Vertical Pattern* setting (Register 92h). Signals from adjacent pixels are summed with the current pixel signal if the *Z-Matrix Enable* bit (Register 92h) is set.

The time to sample and convert one sub-array column (sixteen pixels) is defined by the *Column Scan Period* setting (Register 8Fh). Imaging continues across the sub-array until all 128 columns have been sampled. An additional column scan interval occurs between the last column in a sub-array and the start of the next sub-array.

After the last column in the last sub-array has been sampled, the AF-S2 switches back to *Detect* mode. The finger detection output is ignored for 32µs to allow the excitation generator time to switch back to the *Detect* settings for frequency and amplitude. The finger detection output is then sampled for another 96µs. If the output remains active, another image scan begins (after the conditions ready to being a scan are met).

During this time, the Authentication Word (nine bytes including a header) and register settings used for that image (64 bytes) are sent to the host. Since the next image scan does not start until after the communication port is idle, there may be longer than 128µs between image scans depending on the baud rate setting.

If the finger detection output is not active when it is rechecked at the end of a scan, the array is powered down and the sensor reverts back to checking for a finger at the programmed detection rate.

If the conditions to begin a scan are not met within 100ms, the sensor switches back to *Detect* mode and checks for a finger present. If a finger is present, the timeout will be restarted. If finger is not present, the array will be powered down and the sensor will return to the finger detection state.

The *TxEnable* input (Pin 15) can be used to throttle the serial data from the chip during imaging. In addition to internal buffering that can store two columns worth of data, the image scan can be paused if the input buffer is not ready to accept data. This allows unlimited throttling with no loss of image data.

The *ChipSelect* input (Pin 12) can be used to place the chip in a low power mode. This is done by disabling the internal clock. The control also resets the image control logic so that power to the array and the excitation generator are turned off. Internal control register settings are retained. The *ChipSelect* input, when inactive, also places *DataOut* (Pin 48) in a high impedance state.

New Features in AF-S2

Image Scan Pausing

The AF-S2 will automatically pause an image scan to prevent loss of image data. *TxEnable* (Pin 15) can be used to throttle the serial data from the sensor to avoid data overrun on the host side. In previous versions of the sensor, asserting *TxEnable* for too long a time (that is, greater than the difference between the column scan period and the time to send eight bytes of data) would cause loss of image data. The host would have to recognize this data loss and potentially discard the image (since the lost column could be anywhere in the row).

The AF-S2 will pause the image scan when the buffer for data from the A/D is full. This allows *TxEnable* to throttle serial data from the chip without any loss of image data.

A valuable by-product of this feature is that the column scan rate can be increased to allow maximum usage of the serial channel from the chip.

By setting the column scan period to the next smaller value, the column scan will run at the maximum rate sustainable by the serial channel. This allows faster frame rates. The following table shows the results (assuming that the host can accept all the data without throttling).

Table: Frame Timing

Baud Rate	Column Period Setting	Image Frame Time	Send Data Time	Max Frame Rate
115.2 Kbps	512µs	528 ms	711.8 ms	1.4 fps
460.8 Kbps	128µs	132 ms	177.9 ms	5.6 fps
921.6 Kbps	64µs	66 ms	89.0 ms	10.2 fps
2 MBps	32µs	33 ms	41.0 ms	24.4 fps

Since the image scan is paused by lengthening the time the column scan clock is LOW in 8µs steps, the phase relationships of all control signals remain the same. When the scan clock is LOW, the only function being performed is A/D conversion. The times allocated for DCRST, signal integration, and SAMP remain unaffected.

This feature can be disabled by setting Bit 5 (*Scan Pause Enable*) in Register 80h.

Column Clock Duty Cycle Control

The column clock has a period controlled by the *Column Scan Period* setting in Register 8Fh. In earlier revisions of the sensor, this clock had a fixed 50% duty cycle. A portion of the time the clock is HIGH is allocated to DCRST and SAMP (1/16 of the period for each) with the remainder used to integrate the signal from the pixel demodulator (3/8 of the period).

In the AF-S2, different duty cycles can be selected. These are controlled by the *Column Duty Cycle* setting in Register 81h. The alternate settings can provide increased integration time for a given column-scan period as shown in the following table. The DCRST and SAMP columns show the duration of the DC restore and sample pulses, while the INT column shows the signal integration time.

Table: Column Processing Timing

Column Scan Period	'00'			'10'		
	DCRST	INT	SAMP	DCRST	INT	SAMP
64	2	28	2	2	28	2
128	4	56	4	2	92	2
256	8	112	8	2	220	2
512	16	224	16	2	476	2
1024	32	448	32	2	988	2
2048	64	896	64	2	2012	2

1. All values in this table are expressed in microseconds (µs).
2. All other combinations of variables will result in a NOOP.

Histograms

The graphical representation of scanned fingerprint information in the form of a histogram is a useful tool for the adjustment of the controls provided in the registers.

Earlier revisions of the sensor only provided digitized pixel data as the output during imaging. The AF-S2 includes on-chip histogramming and can provide as output image data, histogram data, or both.

A potential application of this feature is to use the histogram-data-only mode to validate or adjust any of the control register settings. Since this allows fast frame rates at any baud rate, the time needed to adjust sensor registers to obtain the best image will be greatly reduced.

Many of the histogram controls are programmable. Bit 4 (*Histogram Full Array*) in Register 80h controls how many pixels are included in the histogram. When this bit is low, only the center 64 x 64 square (4,096 pixels) is included in the histogram. When high, the whole 128 x 128 array (16,384 pixels) is included. An important point is that the histogram counters are 14-bit, with a range of 0 – 16,383. The histogram counters stick at their maximum count, so in full array mode a count of 16,383 could mean that either 16,383 or 16,384 pixels are at that value. The correct value is easily determined

by looking at the values of the other bins. If there are no pixels in any of the other bins, the true value is 16,384.

Bit 0 (*Histogram Each Row*) in Register 93h controls when the histogram values are returned. When this bit is low, the histogram message is sent once (after the image data and Authentication Word if image data is enabled). When high, a histogram message is sent at the end of each row. The histogram is cumulative, so the message sent at the end of the second row includes pixel values from the first and second row. The histogram counters are only reset at the start of an image frame.

Histogram Data Format

When the histogram message is enabled, it can be sent either once per image or once per row. When sent once per image, it will be sent after the Authentication Word but before the register values. When sent after each row, the histogram for the last row will be sent before the Authentication Word (it will always immediately follow the pixel data). The histogram message is preceded by header byte DEh.

The header is followed by the counts for each of the bins representing possible pixel values. Bin 0 (the number of pixels whose value is 0) is sent first as two bytes. The first byte has the lower seven bits and the second byte has the upper seven bits. This is followed by the counts for the remaining bins.

In the mode where the whole array is included in the histogram, the maximum count value needed if all the pixels were at the same value is 16,384, which requires 15 bits. Since each of the bins are sized at fourteen bits, the counter will stick at the maximum value (16,383) instead of rolling over.

Table: Byte v. Bin

BYTE	DATA (D6 – D0)
1	Header (DEh)
2	Bin0 [6:0]
3	Bin0 [13:7]
4	Bin1 [6:0]
5	Bin1 [13:7]
6	Bin2 [6:0]
|	|
16	Bin7 [6:0]
17	Bin7 [13:7]

Start/Stop Row Controls

The start and stop sub-arrays used during imaging are programmable in Register 89h. The three-bit sub-array counter starts on the sub-array set by the start value (*Start Row*), and stops after the sub-array set by the end value (*End Row*). The counter wraps around - for example, starting at Sub-array 2 and stopping at Sub-array 1 gives a sequence of 2-3-4-5-6-7-0-1. This is the default scanning order.

This also allows images less than the full array size to be obtained. For example, an image from only the four center sub-arrays could be obtained by setting the *Start Row* to 2 and the *End Row* to 5. In this way, images could be acquired at a frame rate double that of using the full array.

Hardware Interface Details

IC Pin Assignments

Figure: AF-S2 Pinout

Pin	Mnemonic	Pin	Mnemonic	Pin	Mnemonic	Pin	Mnemonic
1	VDDD	**18**	DriveRing	**35**	VDDD	**52**	DriveRing
2	VSSD	**19**	no connect	**36**	VSUB	**53**	no connect
3	VSSA	**20**	no connect	**37**	VDDA	**54**	no connect
4	VDDA	**21**	FingerPlate	**38**	VDDD	**55**	PLLEnable#[2]
5	VDDD	**22**	FingerExcite	**39**	VSSD	**56**	BaudSelect3[1]
6	VSSD	**23**	VSSD	**40**	VSSA	**57**	Reset#[3]
7	VSSA	**24**	VDDDon	**41**	VDDA	**58**	ChargePump
8	VDDA	**25**	VDDAon	**42**	Out0[4]	**59**	FingerDrive
9	no connect	**26**	VSSA	**43**	Out1[4]	**60**	VDDAon
10	no connect	**27**	VSUB	**44**	Xout	**61**	VSSA
11	FingerDetect#	**28**	VDDA	**45**	Xin	**62**	VSUB
12	ChipSelect	**29**	VSSA	**46**	VSSD	**63**	VDDA
13	BaudSelect1[1]	**30**	VSSD	**47**	VDDDon	**64**	VSSA
14	BaudSelect2[1]	**31**	VDDD	**48**	DataOut	**65**	VSSD
15	TxEnable	**32**	VDDA	**49**	DataIn	**66**	VDDD
16	no connect	**33**	VSSA	**50**	Out2[4]	**67**	VDDA
17	no connect	**34**	VSSD	**51**	Out3[4]	**68**	VSUB

1. Pin has an internal 20K pull-up.
2. Pin has an internal 20K pull-down.
3. Pin has an internal 50K pull-up.
4. Open drain outputs, capable of sourcing 5ma.

Device Level Interface

Table: Serial Interface Signals

SIGNAL NAME	PIN	PIN TYPE	DRIVER TYPE	FREQ MHZ	DESCRIPTION
BaudSelect3 **BaudSelect2** **BaudSelect1**	56 14 13	I I I	CMOS CMOS CMOS	N/A N/A N/A	Serial I/O data rate and format selection: *BaudSelect 1-3* = RATE 000 = 187.5Kbps NRZ 001 = 230.4Kbps NRZ 010 = 375.0 Kpbs NRZ 011 = 750.0 Kbps NRZ 100 = 2Mbps Man 101 = 115.2Kbps NRZ 110 = 460.8 Kpbs NRZ 111 = 921.6 Kbps NRZ
TxEnable	15	I	CMOS	N/A	Transmit Enable. HIGH to enable sending serial data to host.
DataIn	49	I	TTL	2	Serial input data from host. Data rate and format selected via *BaudSelect1-3*.
DataOut	48	B	CMOS	2	Serial output data from AF-S2. Data rate and format selected via *BaudSelect1-3*.

For all data rates and formats, the data is formatted using a standard asynchronous protocol. The idle state of the line is HIGH. Each data byte sent is preceded by a LOW start bit and followed by a HIGH stop bit. Each eight-bit byte is sent Least Significant Bit (LSB) first. There is no parity bit.

System Timing Interface

Table: System Timing Interface Signals

Signal Name	Pin	Pin Type	Driver Type	Freq MHz	Description
Xin	45	I	CMOS	16	Input from crystal or oscillator
Xout	44	O	CMOS	16	Output to crystal
ChipSelect	12	I	CMOS	N/A	When LOW, forces the internal clock buffer output low. HIGH for normal operation
Reset#	57	I	CMOS	N/A	Master Reset input, active low. When LOW, the sensor is held in reset mode

Excitation Interface

Table: Excitation Interface Signals

Signal Name	Pin	Pin Type	Driver Type	Freq. MHz	Description
FingerDetect#	11	O	CMOS	N/A	Goes LOW when a finger is detected
FingerDrive	59	O	Ana	2	Internally-generated Drive Ring excitation signal
FingerExcite	22	O	Ana	2	Internally-generated Finger Plate excitation signal
FingerPlate	21	I	Ana	2	Internal signal connection to Finger Plate
ChargePump	58	O	Ana	4	Charge Pump Filter for Phase Lock Loop
DriveRing	18, 52	I	Ana	2	Internal signal connection to Drive Ring

Power Supply

Table: Power Supply Signals

Signal Name	Pin Number	Description
VDDDon	24, 47	Digital Power
VDDD	1, 5, 31, 35, 38, 66	Switched Digital Power
VSSD	2, 6, 23, 30, 34, 39, 46, 65	Digital Ground
VDDA	4, 8, 28, 32, 37, 41, 63, 67	Switched Analog Power
VSSA	3, 7, 26, 29, 33, 40, 61, 64	Analog Ground

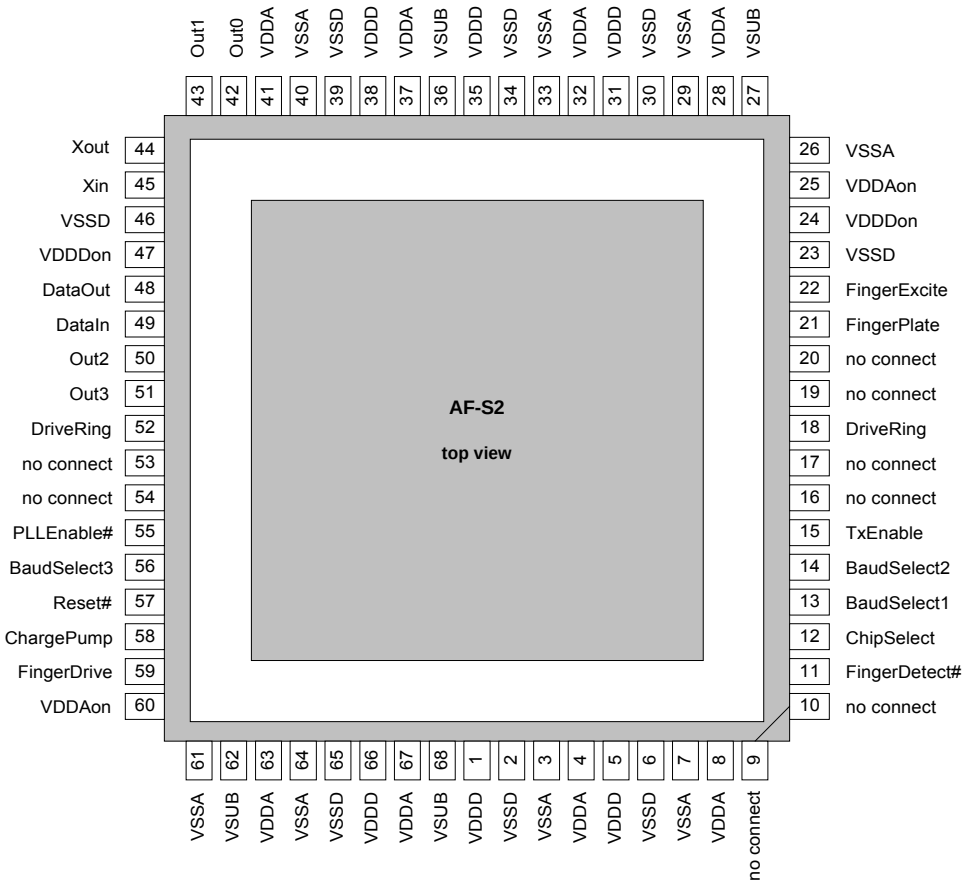
SIGNAL NAME	PIN NUMBER	DESCRIPTION
VDDAon	25, 60	Analog Power
VSUB	27, 36, 62, 68	Substrate Ground

Packaging Information

Form Factor

The AF-S2 is packaged in an industry-standard 68-pin PLCC (Plastic Leadless Chip Carrier) format.

Figure: AF-S2 Pin Configuration



Package Markings

The package branding requirements are detailed in AuthenTec specification PD-10001-401. Contact AuthenTec's Application Engineering Department at **apps@authentec.com** for the latest product information.

Reflow and Storage conditions

Reflow process requirements

Thermal ramp	Ideal thermal ramp is 3°C/37°F per second. Maximum thermal ramp is less than 6°C/74°F per second.
Preheat	Preheat to 95°C/203°F +/- 10°C/50°F for 70 +/- 50 seconds.
Peak temperature	240°C/464°F
Time within 5°C/41°F of peak temperature	10 - 20 seconds

Notes:

- The AF-S2 PLCC package uses Ni/Pd/Au-plated leadframes.
- Special reflow conditions may apply for lead-free solder systems.
- The AF-S2 meets MRT classification moisture sensitivity, Level 3.
- Preferred storage conditions: less than 30°C/86°F and 60% relative humidity.

Environmental Parameters

Maximum Operating Conditions

If the AF-S2 sensor is operated in conditions that exceed the ranges listed in the following tables, significant loss of performance and reliability may be experienced, and damage to the device may result.

Table - Maximum Operating Range

SYMBOL	PARAMETER	MIN	MAX	UNITS
V_{CC}	Supply Voltage	-0.5	6.0	V
V_I	Input Voltage	-0.5	V_{CC}+.5	V
V_0	Output Voltage	-0.5	V_{CC}	V
I_{IK}	Input Clamp Current $V_I < V_{SS}$ of $V_I > V_{CC}$		±20	mA
I_{OK}	Output Clamp Current $V_O < V_{SS}$ of $V_O > V_{CC}$		±20	mA
T_{STG}	Storage Temperature	-65°C -85°F	150°C 302°F	
Latch-Up	Latch-Up Immunity (I/O pins)	±250		mA

Recommended Operating Conditions

Table - Recommended Operating Conditions

MNEMONIC	PARAMETER	MIN	TYP	MAX	UNITS
V_{cc}	Supply voltage	4.5	5	5.5	V
V_i	Input voltage	0		V_{cc}	V
V_o	Output voltage	0		V_{cc}	V
V_{ih}	High-level input voltage	3.3		V_{cc}	V
V_{il}	Low-level input voltage	0		1.6	V
T_t	Input transition (rise and fall) time	0		3	ns
T_j	Junction temperature range (recommended)	-20°C -4°F		45°C 113°F	
T_j	Junction temperature range (maximum)	-20°C -4°F		70°C 158°F	

Warning

The AF-S2 remains fully operational in junction temperature regimes that are high enough to be potentially uncomfortable for the user.

For reasons of safety and protection, AuthenTec reference designs include circuitry that serves to manage the junction temperature by controlling the supply current. If the hardware developer elects not to use the AuthenTec-provided control circuit design, it will then be essential that an equivalent design be developed and implemented.

DC Electrical DC Characteristics

Table: Direct Current Characteristics

MNEMONIC	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{oh}	High-level output voltage	I_{oh} = 2mA	V_{cc}- 0.3			V
V_{ol}	Low-level output voltage	I_{oh} = 2mA			0.3	V
V_t	Positive-going threshold voltage		0.8		2	V
V_{hys}	Hysteresis (V_{t+} - V_{t-})			0.4		V
I_{il}	Low- level input current	$V_i = V_{il}$ (min)			±1	µA
I_{ih}	High-level input current	$V_i = V_{ih}$ (max)			±1	µA
I_{oz}	High-impedance-state output current				±20	µA
I_{cc} (scan)	Supply current	Finger on sensor		70	100	mA
I_{cc} (idle)	Supply current	Waiting for finger		27.5	35	mA
I_{cc} (sleep)	Supply current	ChipSelect = 0 Input held quiescent		20.0	200	µA

Clock Generation and Distribution

The input is clocked at 16 MHz, either generated from a crystal using an on-board oscillator or driven from an external source.

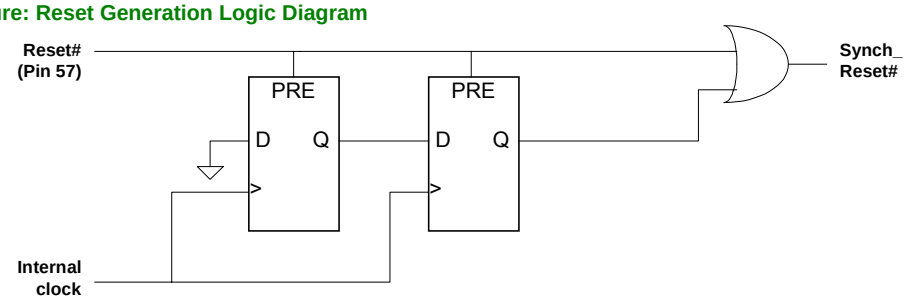
An internal phase lock loop (PLL) multiplies the input frequency by two to produce an internal 32 MHz clock. This clock is used for the majority of the digital logic. The ring counters used to enable power to row and column under-pixel amplifiers are clocked by the column scan clock.

The internal PLL can be bypassed such that the internal logic is clocked at a rate twice that of *Xin* using a digital frequency doubler. This allows the elimination of an external charge pump filter which would otherwise be required.

Reset Strategy

The internal reset state is exited when the external hardware reset pin is released. The internal reset is released after the clock begins operation, thus producing an internal synchronous reset release.

Figure: Reset Generation Logic Diagram



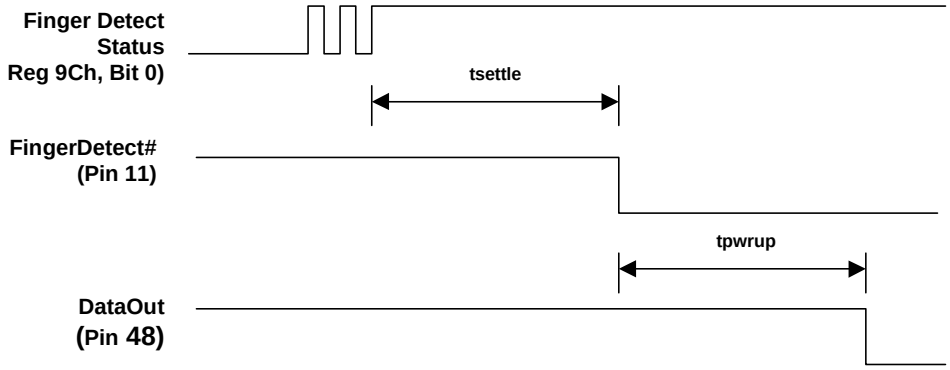
There are also resets generated via the serial interface. “Master Reset” is used to synchronously reset the AF-S2. “Ops Reset” is used to synchronously reset the scan circuitry and update the output registers from buffer registers.

Operational Timing

Image Scan Timing

When a finger is detected on the sensor matrix, the array is powered ON and the AF-S2 begins sending fingerprint image data. The following diagram shows the timing associated with this process.

Figure: Image Scan Timing Diagram



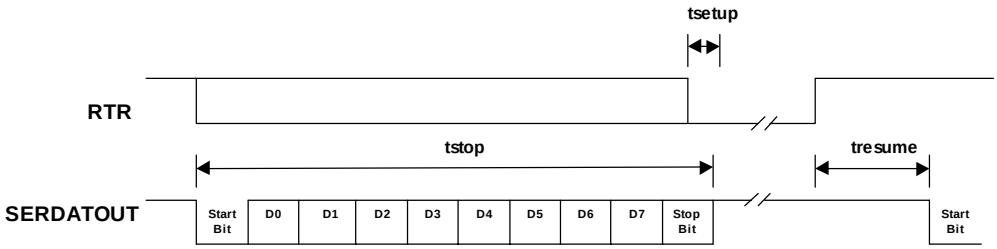
Finger Detect Status is the output of the on-chip finger detector. The ability to detect a finger is dependent on the settings for *Cap* (Register 99h), *Res* (Register 9Ah), *Detect Drive* (Register 8Bh), *Detect Frequency* (Register 98h), and *Drive Bias* (Register 98). Assuming that these registers are set correctly, *Finger Detect Status* will go active after a finger is placed on the sensor. After the *Finger Detect Status* signal has stabilized in the HIGH state, a settling timer (*tsettle* in the preceding diagram) is started.

The finger settling delay is programmable over a range from 31.25ms to 250ms. The settling delay time is reset in the event that *Finger Detect Status* is sampled LOW. After the settling time, the array power is turned ON and a fixed power-up delay period of 32.768ms begins, after which imaging is started (assuming that the conditions necessary for scanning are met). Image data will begin to be sent one column scan period later.

TxEnable Response

The Transmit Enable, *TxEnable* (Pin 15) input can be used to throttle the data output from the chip. The following diagram shows the timing associated with the disabling of the Transmit Enable facility.

Figure: RTR Response Timing Diagram



The *DataOut* circuitry in the AF-S2 consists of a one-byte buffer that feeds an output shift register. The *TxEnable* input is sampled whenever the output shift register is empty, and the shift register is not loaded until *TxEnable* is active. As long as TxEnable is de-asserted more than 40 nanoseconds before the end of the stop bit (*tsetup* in the preceding diagram), data transmission will stop at the end of the current byte. *DataOut* begins clocking out a start bit 125 nanoseconds after *TxEnable* is re-asserted (*tresume* in the preceding diagram).

Downward Compatibility

TxEnable pauses the scan if the internal buffers are not ready to send data. This feature can be disabled (Register 80h, Bit 5 “Scan Pause Disable”) so that column scan timing is not altered and these conditions instead cause loss of image data.

The amount of time that *TxEnable* can be de-asserted will then be limited by the column scan period setting and the baud rate. If *TxEnable* is de-asserted for more than the difference between the two column scan periods and the time to send 16 bytes serially, image data will be lost.

This facility is available for downward compatibility with previous designs – we do not recommend its use for new development.

ChipSelect Response

The ChipSelect input (Pin 12) can be used to put the AF-S2 in a low-power state. It does this by powering-down the internal phase-lock loop so the clock is not running. After ChipSelect is brought HIGH, approximately 500µs must be allowed for the oscillator to start up and the PLL to stabilize prior to attempting to communicate with the AF-S2.

Software Interface Details

Register Map

The following table shows the registers of the AS-S2 and their reset values. Registers that affect imaging are buffered so that they do not change in the middle of a scan. Data is written to the buffer registers using the internal serial interface.

The buffer registers are transferred to output registers at the start of each image scan, or at the start of each detection cycle, or when an *Ops Reset* occurs.

Table: Sensor Register Summary

Cmd	D6	D5	D4	D3	D2	D1	D0	Rst
RSTCTRL								
80h	Reserved	Scan Pause Disable	Histogram Full Array	Histogram Enable	Image Disable	Ops Reset[1]	Master Reset[1]	00h
BITCTRL								
81h	Column Duty Cycle [1]	Column Duty Cycle [1]	Reserved	Scan Trigger	Loopback	Read Registers[1]	Continuous Scan	01h
CHWD1								
82h	Reserved	Reserved	Reserved	Challenge Word [31][1]	Challenge Word [30][1]	Challenge Word [29][1]	Challenge Word [28][1]	00h
CHWD2								
83h	Challenge Word [27][1]	Challenge Word [26][1]	Challenge Word [25][1]	Challenge Word [24][1]	Challenge Word [23][1]	Challenge Word [22][1]	Challenge Word [21][1]	00h
CHWD3								
84h	Challenge Word [20][1]	Challenge Word [19][1]	Challenge Word [18][1]	Challenge Word [17][1]	Challenge Word [16][1]	Challenge Word [15][1]	Challenge Word [14][1]	00h
CHWD4								
85h	Challenge Word [13][1]	Challenge Word [12][1]	Challenge Word [11][1]	Challenge Word [10][1]	Challenge Word [9][1]	Challenge Word [8][1]	Challenge Word [7][1]	00h
CHWD5								
86h	Challenge Word [6][1]	Challenge Word [5][1]	Challenge Word [4][1]	Challenge Word [3][1]	Challenge Word [2][1]	Challenge Word [1][1]	Challenge Word [0][1]	00h
“GP Output Control”								
87h	Reserved	Flash Rate [1]	Flash Rate [0]	Out3	Out2	Out1	Out0	00h
“Pattern Generation”								
88h	Continuous Register Update	PG Enable	Invert Pattern Data	Fix Pattern Data	Pattern Data [2]	Pattern Data [1]	Pattern Data [0]	04h
“Row Scan”								
89h	Reserved	End Row [2]	End Row [1]	End Row [0]	Start Row [2]	Start Row [1]	Start Row [0]	0Ah
CTRL1								
8Ah	Finger Detect Rate [1]	Finger Detect Rate [0]	Data Format [1]	Data Format [0]	Threshold [2]	Threshold [1]	Threshold [0]	64h
CTRL2								
8Bh	Max Resolution	Measure Frequency [2]	Measure Frequency [1]	Measure Frequency [0]	Reserved	Detect Drive [1]	Detect Drive [0]	19h
CTRL3								
8Ch	Demod Phase [6]	Demod Phase [5]	Demod Phase [4]	Demod Phase [3]	Demod Phase [2]	Demod Phase [1]	Demod Phase [0]	06h

Cmd	D6	D5	D4	D3	D2	D1	D0	Rst
CTRL4								
8Dh	FingerSettling Delay [1]	FingerSettling Delay [0]	A/D Ref High [4]	A/D Ref High [3]	A/D Ref High [2]	A/D Ref High [1]	A/D Ref High [0]	3Ah
CTRL5								
8Eh	Reserved	Reserved	A/D Ref Low [4]	A/D Ref Low [3]	A/D Ref Low [2]	A/D Ref Low [1]	A/D Ref Low [0]	07h
CTRL6								
8Fh	Sample/Hold Bias	Analog Channel Bias	Measure Drive [1]	Measure Drive [0]	Column Scan Period [2]	Column Scan Period [1]	Column Scan Period [0]	0Dh
CTRL7								
90h	Finger Detect Filter Disable	Sensor Bias [1]	Sensor Bias [0]	Reserved	Array Power Mode	Array Float	Force Finger Detect	22h
CTRL8								
91h	Reserved	Reserved	Reserved	Sensor Gain 2 [1]	Sensor Gain 2 [0]	Sensor Gain 1 [1]	Sensor Gain 1 [0]	02h
CTRL9								
92h	Reserved	Reserved	Z-Matrix Enable	Z-Matrix Vertical Pattern [1]	Z-Matrix Vertical Pattern [0]	Z-Matrix Horizontal Pattern[1]	Z-Matrix Horizontal Pattern [0]	1Fh
CTRL10								
93h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Histogram Each Row	00h
TREG94								
94h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
TREG95								
95h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
TREG96								
96h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
CTRL11								
97h	Reserved	Reserved	Carrier Null [3]	Carrier Null [2]	Carrier Null [1]	Carrier Null [0]	Carrier Null Enable	10h
CTRL12								
98h	Reserved	Drive Bias [2]	Drive Bias [1]	Drive Bias [0]	Detect Frequency [2]	Detect Frequency [1]	Detect Frequency (0]	03h
CAPADJ								
99h	Cap [6]	Cap [5]	Cap [4]	Cap [3]	Cap [2]	Cap [1]	Cap [0]	7Fh
RESADJ								
9Ah	Reserved	Reserved	Reserved	Reserved	Res [2]	Res [1]	Res [0]	05h
WRITECNT								
9Bh	Write Count [6][2]	Write Count [5][2]	Write Count [4][2]	Write Count [3][2]	Write Count [2][2]	Write Count [1][2]	Write Count [0][2]	00h
STAT								
9Ch	Reserved	Reserved	Manchester Error[2]	Scan Paused[2]	Framing Error[2]	Reserved	Finger Detect Status[2]	00h
DEVID								
9Dh	Device ID [6][2]	Device ID [5][2]	Device ID [4][2]	Device ID [3][2]	Device ID [2][2]	Device ID [1][2]	Device ID [0][2]	30h
REVNUM								
9Eh	Revision Number [6][2]	Revision Number [5][2]	Revision Number [4][2]	Revision Number [3][2]	Revision Number [2][2]	Revision Number [1][2]	Revision Number [0][2]	03h
RUNNUM								
9Fh	Run Series Number [6][2]	Run Series Number [5][2]	Run Series Number [4][2]	Run Series Number [3][2]	Run Series Number [2][2]	Run Series Number [1][2]	Run Series Number [0][2]	00h

1. Write-only
2. Read-only.

The following table is an alphabetical listing showing each of the functional controls of the AF-S2, and the mnemonic and hexadecimal number of the registers in which they are located.

Table: Sensor Functional Controls

CONTROL NAME	REGISTER MNEMONIC	REGISTER NUMBER
A/D Reference High	CTRL4	8Dh
A/D Reference Low	CTRL5	8Eh
Analog Channel Bias	CTRL6	8Fh
Array Float	CTRL7	90h
Array Power Mode	CTRL7	90h
Capacitance	CAPADJ	99h
Carrier Null	CTRL11	97h
Carrier Null Enable	CTRL11	97h
Challenge Word	CHWD1 - 5	83h – 86h
Column Duty Cycle	BITCTRL	81h
Column Scan Period	CTRL6	8Fh
Continuous Register Update	"Pattern Generation"	88h
Continuous Scan	BITCTRL	81h
Data Format	CTRL1	8Ah
Demodulation Phase	CTRL3	8Ch
Detect Drive	CTRL2	8Bh
Detect Frequency	CTRL12	98h
Device Identification	DEVID	9Dh
Drive Bias	CTRL12	98h
End Row	"Row Scan"	89h
Finger Detect Filter Disable	CTRL7	90h
Finger Detect Rate	CTRL1	8Ah
Finger Detect Status	STAT	9Ch
Finger Settling Delay	CTRL4	8Dh
Fix Pattern Data	"Pattern Generation"	88h
Flash Rate	"GP Output Control"	87h
Force Finger Detect	CTRL7	90h
Framing Error	STAT	9Ch
Histogram Each Row	CTRL10	93h
Histogram Enable	RSTCTRL	80h
Histogram Full Array	RSTCTRL	80h
Image Disable	RSTCTRL	80h
Invert Pattern Data	"Pattern Generation"	88h
Loopback	BITCTRL	81h
Manchester Error	STAT	9Ch
Master Reset	RSTCTRL	80h
Maximum Resolution	CTRL2	8Bh
Measure Drive	CTRL6	8Fh
Measure Frequency	CTRL2	8Bh
Operational Reset	RSTCTRL	80h
Out0-Out3	"GP Output Control"	87h
Pattern Data	"Pattern Generation"	88h
PG Enable	"Pattern Generation"	88h
Read Registers	BITCTRL	81h

CONTROL NAME	REGISTER MNEMONIC	REGISTER NUMBER
Resistance	RESADJ	9Ah
Revision Number	REVNUM	9Eh
Run Series Number	RUNNUM	9Fh
Sample/Hold Bias	CTRL6	8Fh
Scan Pause	STAT	9Ch
Scan Pause Disable	RSTCTRL	80h
Scan Trigger	BITCTRL	81h
Sensor Bias	CTRL7	90h
Sensor Gain	CTRL8	91h
Start Row	"Row Scan"	89h
Threshold	RESADJ	9Ah
Write Count	WRITECNT	9Bh
Z-Matrix Enable	CTRL9	92h
Z-Matrix Horizontal Pattern	CTRL9	92h
Z-Matrix Vertical Pattern	CTRL9	92h

Register Descriptions

The following sections provides complete, bit-by-bit descriptions of each addressable register in the AF-S2. Following the title of the particular register, the mnemonic for the register is shown parenthetically, as is the command value used to address the register (in hexadecimal notation) - for example…

Reset Control (RSTCTRL) (80h)

In order to write to a register, a command byte is sent first, indicating which register is to be updated. The contents of a subsequent data byte will be written to the selected register.

All registers receive their reset value after a Power-On Reset (POR), or a Master Reset (Register 80h). For buffered registers, both the buffer and output register receive the reset value.

All register bits are read/write unless otherwise indicated. Reserved bits and write-only bits will always read back as zero. Registers can be written individually but must be read all at once. To read the registers, a *Read Register* command must be sent to the Bit Control Register (Register 81h). The AF-S2 responds with 64 bytes, comprised of 32 register address/data pairs.

Please notice that although eight bits are shown for each register, the registers themselves contain a maximum of seven bits of information since the Most Significant Bit of the value must always be zero.

Note: When writing to registers with reserved bits, only zeros should be written to the reserved register bits to ensure compatibility with successor releases of the AF-S2.

Reset Control (RSTCTRL) (80h)

All bits in this register are write-only.

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Scan Pause Disable	Histogram Full Array	Histogram Enable	Image Disable	Ops Reset	Master Reset
Reset Value	0	0	0	0	0	0	0	0

D6: Reserved

D5: Scan Pause Disable

1 Disable pausing an image scan. If the A/D input buffer is unable to accept data, image data will be lost.

0 Operate normally. If the A/D input buffer is unable to accept data, the scan will pause until the buffer is empty.

D4: Histogram Full Array

1 Include the whole matrix in the histogram.

0 Include only the center 64 x 64 pixel area in the histogram.

D3: Histogram Enable

1 Send histogram data.

0 Do not send histogram data.

D2: Image Disable

1 Do not send end image data.

0 Send image data.

D1: Ops Reset

1 Perform an operational reset. This resets the Master Control circuitry and stops any imaging scan currently in progress. Output registers are loaded from buffer registers. This bit is self-resetting.

D0: Master Reset

1 Perform a Master Reset (same as Power-On Reset). This resets the Master Control circuitry. Output registers and buffer registers are loaded with reset values. This bit is self-resetting.

Bit Control (BITCTRL) (81h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Column Duty Cycle (1)	Column Duty Cycle (0)	Reserved	Scan Trigger	Loopback	Read Registers	Continuous Scan
Reset Value	0	0	0	0	0	0	0	1

D6 – D5: Column Duty Cycle (1 and 0)

Set the duty cycle of the column scan clock.

00 50% duty cycle. SAMP and DCRST pulses are 1/32 of the column scan period.

01 Illegal combination – do not use.

10 T_{LOW} is fixed at 32.0µs. SAMP and DCRST pulses are fixed at 2.0µs.

11 Same as **00**

D4: Reserved

D3: Scan Trigger

1 Perform an image scan. Notice that the *Continuous Scan* bit (D0) must be LOW for this to have any effect. An image scan is performed as soon as a finger is detected. This bit is self-resetting.

A "1" read from this bit location indicates that a single scan is pending.

D2: Loopback

1 Enable Loopback. Data received on *DataIn* (Pin 49) is transmitted on *DataOut* (Pin 48). Loopback takes effect after the data byte that enables it, and lasts until after the data byte that disables it.

0 Disable Loopback.

D1: Read Registers

1 Read the current state of the registers. The request is responded to only if not in Imaging mode. This bit is self-resetting.

The Read request is ignored if Bit 2, *Loopback*, is enabled.

D0: Continuous Scan

1 Perform a continuous scan. Continuous imaging begins as soon as a finger is detected.

0 Perform a controlled scan. Scans are initiated on the rising edge of Bit 3, *Scan Trigger*.

Challenge Word #1 (CHWD1) (82h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Challenge Word [31]	Challenge Word [30]	Challenge Word [29]	Challenge Word [28]
Reset Value	0	0	0	0	0	0	0	0

D6 – D4: Reserved

D3 – D0: Challenge Word [31:28]

All bits in this register are write-only.

Writing to this register alters Bits 31 through 28 of the Challenge Word.

Challenge Word #2 (CHWD2) (83h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Challenge Word [27]	Challenge Word [26]	Challenge Word [25]	Challenge Word [24]	Challenge Word [23]	Challenge Word [22]	Challenge Word [21]
Reset Value	0	0	0	0	0	0	0	0

D6 – D0: Challenge Word [27:21]

All bits in this register are write-only.

Writing to this register alters Bits 27 through 21 of the Challenge Word.

Challenge Word #3 (CHWD3) (84h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Challenge Word [20]	Challenge Word [19]	Challenge Word [18]	Challenge Word [17]	Challenge Word [16]	Challenge Word [15]	Challenge Word [14]
Reset Value	0	0	0	0	0	0	0	0

D6 – D0: Challenge Word [20:14]

All bits in this register are write-only.

Writing to this register alters Bits 20 through 14 of the Challenge Word.

Challenge Word #4 (CHWD4) (85h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Challenge Word [13]	Challenge Word [12]	Challenge Word [11]	Challenge Word [10]	Challenge Word [9]	Challenge Word [8]	Challenge Word [7]
Reset Value	0	0	0	0	0	0	0	0

D6 – D0: Challenge Word [13:7]

All bits in this register are write-only.

Writing to this register alters Bits 13 through 7 of the Challenge Word.

Challenge Word #5 (CHWD5) (86h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Challenge Word [6]	Challenge Word [5]	Challenge Word [4]	Challenge Word [3]	Challenge Word [2]	Challenge Word [1]	Challenge Word [0]
Reset Value	0	0	0	0	0	0	0	0

D6 – D0: Challenge Word [6:0]

All bits in this register are write-only.

Writing to this register alters Bits 6 through 0 of the Challenge Word.

GP Output Control (87h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Flash Rate (1)	Flash Rate (0)	Out3	Out2	Out1	Out0
Reset Value	0	0	0	0	0	0	0	0

D6: Reserved

D5 – D4: Flash Rate

00 Turn ON an external device for continuous display.

01 Flash external device at a rate of 1.0Hz.

10 Flash external device at a rate of 2.0Hz.

11 Flash external device at a rate of 4.0Hz.

D3 – D0: Out3 – Out0

1 Turn ON an external device.

0 Turn OFF an external device.

Pattern Generation (88h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Cont Reg Update	PG Enable	Invert Pattern Data	Fix Pattern Data	Pattern Data (2)	Pattern Data (1)	Pattern Data (0)
Reset Value	0	0	0	0	0	1	0	0

D6: Continuous Register Update

1 Continually update registers from buffers.

0 Update registers only before a *Detect* cycle, before an image scan operation, or when triggered by an *Ops Reset* (Register 80h, Bit 1). This is the default value.

D5: PG Enable

1 Enable pattern generation.

0 Disable pattern generation. This is the default value.

D4: Invert Pattern Data

1 Invert pattern data.

0 Do not invert pattern data. This is the default value.

D3: Fix Pattern Data

1 Fix pattern data. Value depends on D4 and D2 - D0 bits.

0 Pattern data is from a five-bit Pseudo-random Noise (PN) pattern generator.

D2 – D0: Pattern Data

Set the data pattern when in *Fix Pattern Data* (Bit 3) mode. The *Pattern Data* controls are not buffered. Changing a setting during a scan operation changes the data output for that scan “on-the-fly”.

In *PG Enable* (Bit 5) mode, the data is transmitted (in normal mode) in the following repeating 31-byte pattern:

35h, 66h, 64h, 30h, 44h, 52h, 37h, 32h, 10h, 26h, 21h, 57h, 15h, 04h, 17h, 50h, 63h, 46h, 06h, 43h, 24h, 75h, 23h, 03h, 61h, 12h, 72h, 55h, 41h, 70h, 01h

Row Scan (89h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	End Row (2)	End Row (1)	End Row (0)	Start Row (2)	Start Row (1)	Start Row (0)
Reset Value	0	0	0	0	1	0	1	0

D6: Reserved

D5 – D3: End Row

Set the ending row in the sub-array for an image scan operation.

D2 – D0: Start Row

Set the starting row in the sub-array for an image scan operation.

Control #1 (CTRL1) (8Ah)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Finger Detect Rate [1]	Finger Detect Rate [0]	Data Format (1)	Data Format (0)	Thresh-hold (2)	Thresh-hold (1)	Thresh-Hold (0)
Reset Value	0	1	1	0	0	1	0	0

D6 – D5: Finger Detect Rate [6:5]

Set the cyclic rate at which the stimulus source and finger-detection circuitry are turned ON. For all settings (except **11** - Continuous) the stimulus is turned ON for a period of 128µs.

00 Detection cycles occur every 8.192ms (equivalent to 122Hz)

01 Detection cycles occur every 131.072ms (equivalent to 7.63Hz)

10 Detection cycles occur every 1.048 seconds (equivalent to 0.95Hz)

11 Operate continuously. The excitation generation and finger detection circuitry remain ON.

Registers are updated from buffer storage prior to each detection cycle. In *Continuous* mode, registers are updated continuously.

D4 – D3: Data Format

Set the format for image data output.

00 Set image density of three bits per pixel, packed two pixels per byte. This is the default value.

01 Pack image data using all eight bits, so 16 pixels are sent as six bytes. Each row takes 768 bytes.

10 Send image data at the rate of one bit per pixel. Data format is the same as **00** (only six bits used per byte). Each row takes 344 bytes.

11 Send image data at the rate of one bit per pixel and packed eight bits per byte. Three columns are sent as six bytes. Each row takes 258 bytes.

D2 – D0: Threshold

Set the threshold value for one bit per pixel mode. Pixels with A/D values greater than or equal to threshold value are sent as ones.

Control #2 (CTRL2) (8Bh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Max Res	Measure Frequency [2]	Measure Frequency [1]	Measure Frequency [0]	reserved	Detect Drive [1]	Detect Drive [0]
Reset Value	0	0	0	1	1	0	0	1

D6: Maximum Resolution

1 Change the definition of the *Demod Phase* register (8Ch) to a constant resolution (LSB = 2.8125°) and an angular range of 0 – 357.1875°

0 This is the default value.

D5 – D3: Measure Frequency

Set the frequency of the internal excitation generator when in *Measure* mode. Out-of-range settings default to 2.0MHz.

001 Set excitation generator frequency to 125.0KHz

010 Set excitation generator frequency to 250.0KHz

011 Set excitation generator frequency to 500.0KHz

100 Set excitation generator frequency to 1.0MHz

101 Set excitation generator frequency to 2.0MHz

D2: Reserved

D1 – D0: Detect Drive

Set the peak-to-peak voltage level of the excitation generator when in *Detect* mode.

00 Set voltage level to $0.3V_{pp}$

01 Set voltage level to $1.0V_{pp}$

10 Set voltage level to $2.0V_{pp}$

11 Set voltage level to $4.0V_{pp}$

Control #3 (CTRL3) (8Ch)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Demod Phase [6]	Demod Phase [5]	Demod Phase [4]	Demod Phase [3]	Demod Phase [2]	Demod Phase [1]	Demod Phase [0]
Reset Value	0	0	0	0	0	1	1	0

D6 – D0: Demod Phase

Set the phase of the demodulation clock relative to the positive zero crossing of the excitation generator. The Least Significant Bit (LSB) weight (angular step size) is dependent on the stimulus frequency.

A value of “all zeros” sets a 180-degree phase shift. Other values provide a shift of (n-1) times the listed step size. Out-of-range bits are masked off.

STIMULUS FREQUENCY (KHZ)	ANGULAR STEP	VALID RANGE
Maximum Resolution[1]	2.8125°	00h – 7Fh = 0 – 357.1875
2,000	11.25°	00h, 01h – 0Fh = 180, 0 - 157.5
1,000	11.25°	00h, 01h – 0Fh = 180, 0 - 157.5
500	5.625°	00h, 01h – 1Fh = 180, 0 - 168.75
250	5.625°	00h, 01h – 1Fh = 180, 0 - 168.75
125	2.8125°	00h, 01h – 3Fh = 180, 0 - 174.375

1. Maximum resolution is enabled by setting Register 8Bh, Bit 6.

Control #4 (CTRL4) (8Dh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Finger Settling Delay [1]	Finger Settling Delay [0]	A/D Ref High [4]	A/D Ref High [3]	A/D Ref High [2]	A/D Ref High [1]	A/D Ref High [0]
Reset Value	0	0	1	1	1	0	1	0

D6 – D5: Finger Settling Delay

Set the time delay in milliseconds from the moment when a finger is detected on the sensor matrix to when imaging begins.

00 Set time delay to 31.25ms

01 Set time delay to 62.5ms

10 Set time delay to 125.0ms

11 Set time delay to 250.0ms

D4 – D0: A/D Reference High

Set the high reference voltage to the A/D converter. If the A/D Reference High setting is not greater than the A/D Reference Low (Register 8Eh) setting, it will be ignored (to lower both settings, set the A/D Reference Low to its new value first).

Control #5 (CTRL5) (8Eh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	A/D Ref Low [4]	A/D Ref Low [3]	A/D Ref Low [2]	A/D Ref Low [1]	A/D Ref Low [0]
Reset Value	0	0	0	0	0	1	1	1

D6 – D5: Reserved

D4 – D0: A/D Reference Low

Set the high reference voltage to the A/D converter. If the A/D Reference Low setting is not less than the A/D Reference High (Register 8Dh) setting, it will be ignored (to raise both settings, set the A/D Reference High to its new value first).

Control #6 (CTRL6) (8Fh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Sample/ Hold Bias	Analog Channel Bias	Measure Drive [1]	Measure Drive [0]	Column Scan Period [2]	Column Scan Period [1]	Column Scan Period [0]
Reset Value	0	0	0	0	1	1	0	1

D6: Sample/Hold Bias

1 Double the bias current in the sample/hold amplifier.

0 Default value.

D5: Analog Channel Bias

1 Double the bias current in the analog channel amplifier.

0 This is the default value

D4 – D3: Finger Drive Level (Measure)

Set the peak-to-peak voltage level of the stimulus signal when in *Measure* mode.

00 Set the voltage level to 0.3V_{pp}

01 Set the voltage level to 1.0V_{pp}

10 Set the voltage level to 2.0V_{pp}

11 Set the voltage level to 4.0V_{pp}

D2 – D0: Column Scan Period

Set the time used for scanning one column. Out-of-range settings or invalid values default to the 2,048.0-microsecond scan period.

VALUE	COLUMN PERIOD	IMAGE PERIOD	VALID DATA RATES[1]
001	64.0µs	66.016ms	2.0Mbps
010	128.0µs	132.032ms	750.0bps and above
011	256.0µs	264.064ms	375.0Kbps and above
100	512.0µs	528.128ms	187.5Kbps and above
101	1,024.0µs	1.056sec	All
110	2,048.0µs	2.112sec	All

1. Based on normal image data format and no scan throttling.

The maximum frame rate for any column scan period setting will depend on the image period plus the additional time required to send the Authentication Word header and value (nine bytes) and register headers and values (64 bytes).

DATA RATE	ADDITIONAL TIME
115.2Kbps	6.337ms
460.8Kbps	1.584ms
921.6Kbps	792.0µs
2.0Mbps	365.0µs
750Kbps	973.0ms
375.0Kbps	1.946 ms
187.5Kbps	3.893µs
230.4Kbps	365.0µs

Control #7 (CTRL7) (90h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Finger Detect Filter Disable	Sensor Bias [1]	Sensor Bias [0]	reserved	Array Power Mode	Array Float	Force Finger Detect
Reset Value	0	0	1	0	0	0	1	0

D6: Finger Detect Filter Enable

0 Enable Finger Detect output filter.

1 Disable Finger Detect output filter.

D5 – D4: Sensor Bias

Set the array power level by changing the bias levels for the under-pixel amplifiers.

00 Set the under-pixel amplifiers to 2.5µA.

01 Set the under-pixel amplifiers to 5.0µA.

10 Set the under-pixel amplifiers to 8.0µA.

11 Set the under-pixel amplifiers to 10.0µA.

D3: Reserved

D2: Array Power Mode

1 Array Power is always ON.

0 Array Power is switched ON only when a finger has been detected on the sensor matrix.

D1: Array Float

1 Float the pixel sensor plates when they are not activated by the digitization circuitry.

0 Connect the pixel sensor plates to Pin 21 “FingerPlate” when they are not activated by the digitization circuitry.

D0: Force Finger Detect

1 Operate continuously in *Measure* mode.

0 Enter *Measure* mode only when a finger is detected on the sensor matrix.

Control #8 (CTRL8) (91h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Sensor Gain 2 [1]	Sensor Gain 2 [0]	Sensor Gain 1 [1]	Sensor Gain 1 [0]
Reset Value	0	0	0	0	0	0	1	0

D6 – D4: Reserved

D3 – D2: Sensor Gain #2

Set the gain rate multiple in the second stage of the analog channel.

00 Set a gain rate of 2 times.

01 Set a gain rate of 4 times.

10 Set a gain rate of 8 times.

11 Set a gain rate of 16 times.

D1 – D0: Sensor Gain #1

Set the gain rate multiple in the first stage of the analog channel.

00 Set a gain rate of 2 times.

01 Set a gain rate of 4 times.

10 Set a gain rate of 8 times.

11 Set a gain rate of 16 times.

Control #9 (CTRL9) (92h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Z-Matrix Enable	Z-Matrix Vertical Pattern [1]	Z-Matrix Vertical Pattern [0]	Z-Matrix Horizontal Pattern [1]	Z-Matrix Horizontal Pattern [0]
Reset Value	0	0	0	1	1	1	1	1

D6 – D5: Reserved

D4: Z-Matrix Enable

1 Enable signals from adjacent pixels to be summed

0 Disable summing from adjacent pixels

D3 – D2: Z-Matrix Vertical Pattern

Set the number of pixels, arranged vertically in adjacent sub-array rows, whose under-pixel amplifiers are turned on along with the active pixel. This setting defines the vertical dimension of a rectangle (or "cloud" of pixels), centered on the active column, whose horizontal dimension is set by Bits D1 – D0, *Z-Matrix Horizontal Pattern*. Since the height of a sub-array is 16 pixels, this range describes the extent to which the cloud overlaps the adjacent sub-arrays. For a graphic depiction of this setting, refer to the illustration following the horizontal pattern description.

00 Set the range of active elements to be ±1 pixel.

01 Set the range of active elements to be ±2 pixels.

10 Set the range of active elements to be ±3 pixels.

11 Set the range of active elements to be ±4 pixels.

D1 – D0: Z-Matrix Horizontal Pattern

Set the number of pixels, arranged horizontally in adjacent columns of a sub-array, whose under-pixel amplifiers are turned on along with the amplifiers of the pixels in the active column. This setting defines the horizontal dimension of a rectangle (or "cloud" of pixels), centered on the active pixel, whose vertical dimension is set by Bits D3 – D2, *Z-Matrix Vertical Pattern*. For a graphic depiction of this setting, refer to the following illustration:

00 Set the range of active elements to be ±2 pixels, for a total width of five pixels:

o●●•●●o

01 Set the range of active elements to be ±4 pixels, for a total width of nine pixels:

o●●●●•●●●●o

10 Set the range of active elements to be ±6 pixels, for a total width of 13 pixels:

o●●●●●●•●●●●●●o

11 Set the range of active elements to be ±8 pixels, for a total width of 17 pixels:

o●●●●●●●●•●●●●●●●●o

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During a scan the under-pixel amplifiers of all 16 pixels (•) in a given column are activated at once, as are those of certain adjacent pixels (●) specified by the *Z-Matrix Vertical Pattern* and *Z-Matrix Horizontal Pattern* bits.

The Z-Matrix pattern shown here is the minimum "cloud" (90 pixels) produced by **00** matrix settings – ±1 pixel in the vertical dimension and ±2 pixels in the horizontal. Notice that this vertical setting results in an overlap of one pixel each into the sub-array above and below the currently active one.

Control #10 (CTRL10) (93h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	reserved	reserved	reserved	reserved	reserved	reserved	Histogram Each Row
Reset Value	0	0	0	0	0	0	0	0

D6 – D1: Reserved

D0: Histogram Each Row

This bit is ignored if the histogram function is not enabled (Register 80h, Bit 3).

1 Send a histogram message at the end of each row.

0 Send a histogram message after the image scan operation is complete.

Test 94 (TREG94) (94h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset Value	0	0	0	0	0	0	0	0

D6 – D0: Reserved

Test 95 (TREG95) (95h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset Value	0	0	0	0	0	0	0	0

D6 – D0: Reserved

Test 96 (TREG96) (96h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Reset Value	0	0	0	0	0	0	0	0

D6 – D0: Reserved

Control #11 (CTRL11) (97h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Carrier Offset Null (3)	Carrier Offset Null (2)	Carrier Offset Null (1)	Carrier Offset Null (0)	Carrier Offset Null Enable
Reset Value	0	0	0	1	0	0	0	0

D6 – D5: Reserved

D4 – D2: Carrier Offset Null

Add a negative voltage to the signal prior to the A/D conversion. The following table shows the voltages associated with each setting: V_{DAC} is the DAC output voltage and *Output Step Voltage* is the voltage summed with the signal.

VALUE	V_{DAC}	OUTPUT STEP VOLTAGE
0000	0.25	-3.8
0001	0.5	-3.5
0010	1.0	-3.0
|	|	|
1110	3.5	-0.5
1111	4.0	0.0

D1 – D0: Carrier Offset Null Enable

1 Enable carrier null.

0 Disable carrier null.

Control #12 (CTRL12) (98h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Drive Bias [2]	Drive Bias [1]	Drive Bias [0]	Detect Frequency [2]	Detect Frequency [1]	Detect Frequency [0]
Reset Value	0	0	0	0	0	0	1	1

D6: Reserved

D5 – D3: Drive Bias

Set the level, expressed in milliamperes, of the excitation supply current. Out-of-range settings default to **100**.

000 Set supply current to 1.6mA.

001 Set supply current to 2.8mA.

010 Set supply current to 5.0mA.

011 Set supply current to 9.0mA.

100 Set supply current to 16.5mA.

D2 – D0: Detect Frequency

Set the frequency, expressed in kilohertz, of the stimulus signal when in *Detect* mode. Out-of-range settings default to **101**.

001 Set stimulus frequency to 125.0KHz.

010 Set stimulus frequency to 250.0KHz.

011 Set stimulus frequency to 500.0KHz.

100 Set stimulus frequency to 1.0MHz.

101 Set stimulus frequency to 2.0MHz. This is the default value for out-of-range settings.

Sensitivity Capacitance Adjust (CAPADJ) (99h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Cap [6]	Cap [5]	Cap [4]	Cap [3]	Cap [2]	Cap [1]	Cap [0]
Reset Value	0	0	0	0	0	0	0	0

D6 – D0: Cap

Select the capacitance value to be used in the finger detection circuit. An "all zeros" value provides the lowest capacitance value (the most sensitivity).

0000000 Set capacitance value to 93.75ff.

0000001 Set capacitance value to 184.35ff.

▼ ▼

1111111 Set capacitance value to 11.6pf.

Sensitivity Resistance Adjust (RESADJ) (9Ah)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Res [2]	Res [1]	Res [0]
Reset Value	0	0	0	0	0	0	0	0

D6 – D3: Reserved

D2 – D0: Res

These bits select the resistance value used in the finger detection circuit. An "all-ones" value provides the highest resistance value (the most sensitivity).

111 Select reference resistance of 4.0KΩ.

110 Select reference resistance of 2.0KΩ.

10x Select reference resistance of 1.0KΩ.

0xx Select reference resistance of 500.0Ω.

In which **x** denotes a "don't care" value.

Write Count (WRITECNT) (9Bh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Write Count [6]	Write Count [5]	Write Count [4]	Write Count [3]	Write Count [2]	Write Count [1]	Write Count [0]
Reset Value	0	0	0	0	0	0	0	0

D6 – D0: Write Count

All bits in this register are read-only.

This register is a free-running counter that counts the number of register writes. The counter increments when a data byte is received and the preceding command byte was in the range 80h – 9Fh. The counter is reset by a Power-On Reset or a Master Reset.

Status (STAT) (9Ch)

All bits in this register are read-only.

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Manchester Error	Scan Paused	Framing Error	Reserved	Finger Detect Status
Reset Value	0	0	0	0	0	0	0	0

D6 – D5: Reserved

D4: Manchester Error

HIGH indicates that a Manchester Error (constant level for > 1.25-bit period) occurred since the last time the registers were read. These bits are cleared after the register is read.

D3: Scan Paused

HIGH indicates that a scan has paused because the input buffer is full, and thus is unable to accept A/D data. This bit is cleared after the register is read. The *Scan Paused* bit is also set during histogram messages, because the column scan clock is paused to allow the histogram message to complete.

D2: Framing Error

HIGH indicates that a Framing Error (the stop bit was not a logical 1) occurred since the last time the registers were read. This bit is cleared after register is read.

D1: Reserved

D0: Finger Detect Status

The current state of the Finger On detector.

1 A finger was detected on the sensor matrix.

0 No finger is detected on the sensor matrix.

Device Identification (DEVID) (9Dh)

All bits in this register are read-only.

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Device ID [6]	Device ID [5]	Device ID [4]	Device ID [3]	Device ID [2]	Device ID [1]	Device ID [0]
Reset Value	0	0	1	1	0	0	0	0

D6 – D0: Device ID

Set the Device ID.

Revision Number (REVNUM) (9Eh)

All bits in this register are read-only.

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Revision Number [6]	Revision Number [5]	Revision Number [4]	Revision Number [3]	Revision Number [2]	Revision Number [1]	Revision Number [0]
Reset Value	0	0	0	0	0	0	1	1

D6 – D0: Revision Number

"03h" identifies the sensor as a model AF-S2.

Run Series Number (RUNNUM) (9Fh)

All bits in this register are read-only.

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Run Series Number [6]	Run Series Number [5]	Run Series Number [4]	Run Series Number [3]	Run Series Number [2]	Run Series Number [1]	Run Series Number [0]
Reset Value	0	x	x	x	x	x	x	x

D6 – D0: Run Series Number

Indicates the metal mask revision level for this revision level of the sensor.

Implementation Details

Sensor Control and Imaging

Because of the extremely wide range of possible targets, controlling the AF-S2 in order to obtain good images is an understandably complex task - there is no simple set of register setting that will invariably get adequate results from the fingers of all possible users. Generally, several registers must be modified simultaneously in order to perform appropriate gain control. Depending on the condition of the finger, phase and frequency may also have to be adjusted to get good images. This should only be attempted by designers with a strong understanding of analog feedback control systems.

For most systems, using the existing control-loop code that was developed by AuthenTec is the simplest and most direct way to get a system working. As a starting point for the designer of an analog feedback control system, the following register settings will give a good image for a "normal" finger. Gain control should be added to this in order to adjust for differences in signal strength between fingers.

Table: Register Settings for a “Normal” Finger

REGISTER	VALUE (HEXADECIMAL)
80h	00h
81h	01h
82h	00h
83h	00h
84h	00h
85h	00h
86h	00h
87h	00h
88h	0Ah
89h	38h
8Ah	64h
8Bh	0Ah
8Ch	04h
8Dh	34h
8Eh	0Ch
8Fh	72h
90h	12h
91h	0Bh

REGISTER	VALUE (HEXADECIMAL)
92h	1Fh
93h	00h
94h	00h
95h	00h
96h	00h
97h	14h
98h	1Ch
99h	29h
9Ah	05h

Communication Interface

The Communication Interface in the sensor receives command and data bytes via a serial interface and uses them to update register settings. The registers that affect scanning are buffered. New settings are loaded to buffer registers. The buffer registers are transferred to output registers under control of the serial interface (*Ops Reset*, Register 80h, Bit 1) or the on-chip circuitry which performs register updates prior to scanning.

Register settings can be read over the serial interface using the *Read Registers* bit (Register 81h, Bit 1). During scanning, pixel data is sent over the serial interface along with an Authentication Word (checksum) and a copy of the register settings

Recommended Operation

This section describes in detail some of the operating controls of the sensor and provides recommended settings.

General

The *Drive Bias* setting in Register 98h sets the bias in the excitation generator amplifiers. Too low a value will cause amplifier roll-off and distortion at higher frequencies. The 5mA setting has been found to be adequate for all frequencies.

Drive levels (*Detect Drive* in Register 8Bh and *Measure Drive* in Register 8Fh) below 2.0V generally cause problems with detection, and weak images in *Measure* mode.

Finger Detection

The finger detection threshold is adjusted by changing the reference resistor (Register 9Ah) and capacitor (Register 99h) values. A capacitor setting only slightly higher than the point where the sensor self-triggers is usually adequate to reliably detect the presence of a finger.

Imaging

Under-pixel amplifier *Sensor Bias* (Register 90h) sets the bias in the pixel amplifiers. Too low a level may cause roll-off at higher frequencies. A value of 5.0µA generally works well.

Demod phase (Register 8Ch) should be adjusted for maximum ridge clarity.

The *Analog Channel Bias* and *Sample/Hold Bias* (Register 8Fh) should both be set HIGH.

The *Sensor Gain* values (Register 91h) should be adjusted so the output signal is within the A/D range (1.0V – 4.0V). The A/D reference HIGH and LOW values can then be adjusted so that the HIGH is just above the highest signal, and the low is just below the lowest (non-noise) signal value. The analog channel signal has a noise floor of around 1.0V.

The *Carrier Null* (Register 97h) setting can be used to shift the output signal down. This is useful if there is a strong signal but a small amount of ridge to valley variation.

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