Preliminary

AuthenTec, Inc.
Personal Security for the Real World™

Product Specification
…for the AFS8500 Fingerprint Sensor

Minutiae
047 018 287
106 021 192
070 023 210
053 024 000
073 032 230
108 032 428
091 033 174
058 039 248
108 054 402
125 059 400
099 060 400
070 061 256
048 068 340
065 070 338
104 071 358
115 075 358
041 077 096
123 079 384
063 083 064
053 091 052
028 097 052
084 100 031
050 102 044
103 106 050
117 111 046
104 118 282

Hardware Reference

2241 Rev 1.0a
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Product Specification for the AFS8500 Fingerprint Sensor
2241 Rev 1.0a (28May02)

Table of Contents

INTRODUCTION

The *AFS8500 Product Specification* is a hardware reference manual. It describes in detail the physical organization, operation, interfaces, and internal functionality of the AuthenTec EntréPad™ AFS8500™ fingerprint sensor integrated circuit.

The AFS8500 sensor uses state-of-the-art techniques to capture and transmit a fingerprint from a user to a host computer. Reference Design Kits are available that can assist the developer in producing designs that take advantage of the powerful features of this chip.

Note: This Product Specification may contain preliminary data. Users should be aware that information on AuthenTec's products, the Company, and other matters (including software updates) may be available on the AuthenTec web site at www.authentec.com.

For further information or guidance, contact AuthenTec Application Engineering at apps.authentec.com for the latest product information.

Scope

This hardware specification is intended for the use of hardware designers, software designers, and others who require detailed information about the functionality and operation of the AFS8500 sensor.

Applicability

This edition of the *AFS8500 Product Specification* is release version 1.2. It replaces all preliminary versions with various changes. The material in this document applies only to the AuthenTec AFS8500 sensor.

Conventions

Vector Presentation

For vectors (groups of bits), ordering will always be from MSB to LSB (for example, Pixel_Data[47:0] where bit 47 is the MSB and bit 0 is the LSB).

When vectors that span multiple bytes are transmitted, the lower byte (bits [7:0]) is transmitted first. This applies to pixel data and the authentication word returned after each imaging frame.

Typography and Related Information

Numbers followed by a "b" are in binary notation. Numbers followed by an "h" are in hexadecimal. Signal names are active HIGH unless they are followed by a "*" that indicates the signal is active LOW.

Reference

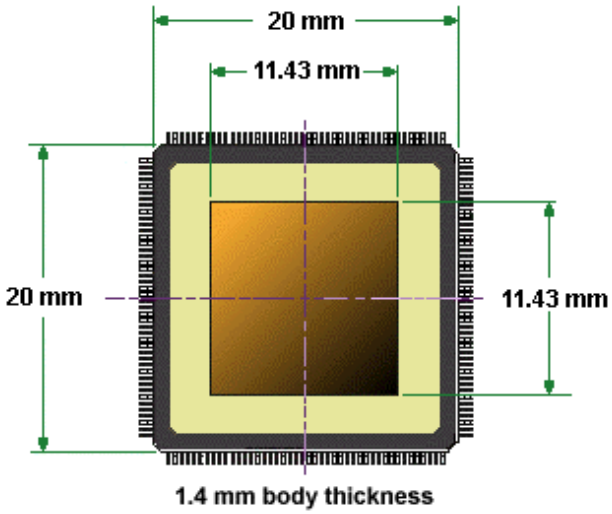
This publication is prepared and presented in accordance with the guidelines and conventions of the *Microsoft Manual of Style for Technical Publications*, Microsoft Press, Redmond WA USA. Other reference material includes the *Chicago Manual of Style*, University of Chicago Press, Chicago IL, and the *IBM Dictionary of Computing*, Information Development, Poughkeepsie NY.

OVERVIEW

Form Factor

The AFS8500 sensor is packaged in a JEDEC-standard 144-pin LQFP (Low-profile Quad Flat Package). Physical dimensions (in millimeters) are shown in the following illustration.

Figure - AFS8500 Dimensions



Functional Summary

The AFS8500 sensor is comprised of a **sensor matrix**, a **drive ring**, and supporting electronics. The purpose of these elements is to detect the presence of a finger placed on the surface of the sensor matrix, and to reliably produce a digital image of the fingerprint. This image must be suitable for processing through AuthenTec, AuthenTec Solution Provider, or third-party software for the purpose of identifying (authenticating) the person associated with the image.

The Sensor Matrix

A fingerprint detection platen, the *sensor matrix*, occupies the center of the chip. This area is 11.43mm (0.45 in) square, and is the actual surface of the integrated circuit die.

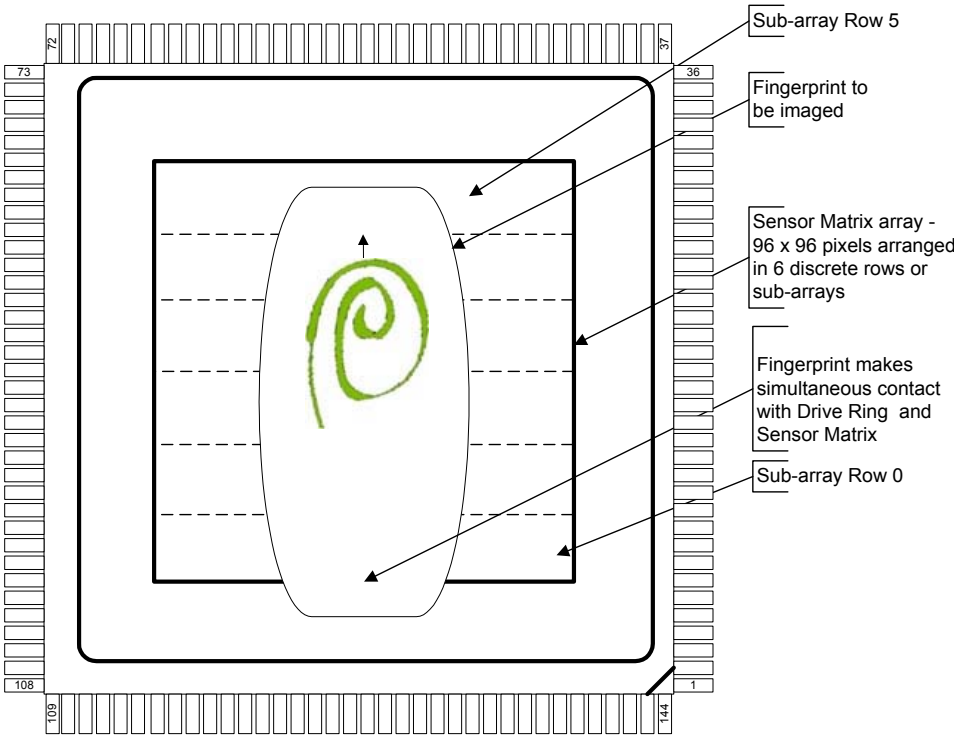
The surface of the *sensor matrix* is treated with a proprietary, advanced ceramic coating, having a Mohs hardness rating of 7+. The purpose of this layer is to protect the exposed IC and to generally resist abrasion and wear.

The *sensor matrix* is comprised of 9,216 individual elements arranged in a 96 x 96 square pattern. It is further organized into six rectangular rows or “sub-arrays”

(numbered 0 through 5), each containing 96 columns of 16 pixels (1,536 elements). With the notched corner of the IC on the lower right (when viewed from the *sensor matrix* side) the sub-array rows are oriented in horizontal bands across the surface with row 0 at the bottom as illustrated below.

Each element in the *sensor matrix* is provided with an under-pixel amplifier, a synchronous demodulator, and a spatial filter node. Scanning each column within an enabled sub-array digitizes the image. A 16 channel multiplexer selects the active column. From the multiplexer each of the 16 pixels in the column of the enabled sub-array is sampled and digitized.

The AFS8500 has two pin-selectable interfaces: Parallel and Serial. For each configuration, the designer must be careful to appropriately tie unused inputs on the package.



The Drive Ring

A rectangular, annular drive ring surrounds the sensor matrix. The *drive ring* is lighter in color than the adjacent chip body and sensor matrix.

The *drive ring* is excited by on-chip direct digital synthesis components that generate a sinusoidal signal. The phase, frequency, and amplitude of this signal are programmatically controlled through the use of the sensor control registers.

Operation

The *sensor matrix* is in effect an array of active antennas that receives the very small signal transmitted by the drive ring. The *drive ring* signal is coupled to the user's finger and is modulated by its passage through the subdermal structure of the finger. The finger must make simultaneous contact with both the sensor matrix and the drive ring (see the preceding illustration) to create a pattern that accurately mimics the configuration of this living skin layer.

Digitizing the multiplexed outputs from one sensor row at a time, in a user-specified programmatic sequence, creates a fingerprint image. The default is from Row 0 through Row 6, wrapping back from Row 6 to Row 0, starting at the rightmost column. The AFS8500 offers the capability of starting and stopping the scan at a user-selectable sub-array. This allows the programmer to establish a strategy for which portion of the fingerprint is to be scanned. A shorter scan can result in quicker settling of Automatic Gain Control (AGC) software and thus a consequent saving in real time.

During imaging, power is applied to a selected column in a selected row, enabling the column to drive an analog channel bus. The analog channel is amplified, integrated, and presented to *sample* and *hold* circuits. The sample and hold outputs are digitized and are then at the selected interface.

Functional Features

Here is a high-level feature list for the AFS8500 fingerprint sensor:

- Programmable finger-on detection rate. The sensor IC remains in idle mode between the 128µs-long finger detection periods. (Register 83h).
- Independent control of stimulus frequency and amplitude for Detection mode. (Register 86h and 87h).
- Independent control of stimulus frequency and amplitude for Measurement mode. (Register 89h and 8Ah).
- Programmable settling delay period to minimize transition to Measurement mode due to noise (Register 83h).
- Automatic transition to Measurement mode after detecting a finger. This feature can be over-ridden so that the AFS8500 remains permanently in Measurement mode (Register 81h).
- Adjustable bias for the under-pixel amplifiers (Register 8Ah).
- Adjustable phase of the demodulation signal relative to the stimulus (Register 8Ch and 8Dh).
- Settable Column Scan period. (Register 88h).

- Settable horizontal and vertical size of the high-pass spatial filter, or disable it (Register 8Bh and 8Fh).
- Adjustable analog channel bias (Register 8Fh) and gain (Register 8Eh).
- Adjustable low (Register 92h) and high (Register 91h) reference voltages for the A/D converter, thus increasing the effective dynamic range of the sensor's A/D converter.
- Programmable Challenge Word for data authentication. The Challenge Word is used along with an embedded word and the pixel data to generate an Authentication Word. The Authentication Word is used to verify that the pixel data is valid information from an AFS8500 sensor (Registers 9Bh through 9Fh).
- On-chip histogramming of the whole array, or just the center 64 x 64 pixels (Register 98h).
- Programmable control over the start and end row and column used for imaging. (Register 93h – 96h).
- Adjustable column scan duty cycle to maximize the time available for A/D signal integration (Register 88h).
- Alternate data representations (Register 97h)…
  - Two three-bit pixels per byte.
  - Eight three-bit pixels per three bytes.
  - Six one-bit pixels per byte.
  - Eight one-bit pixels per byte.

New Features

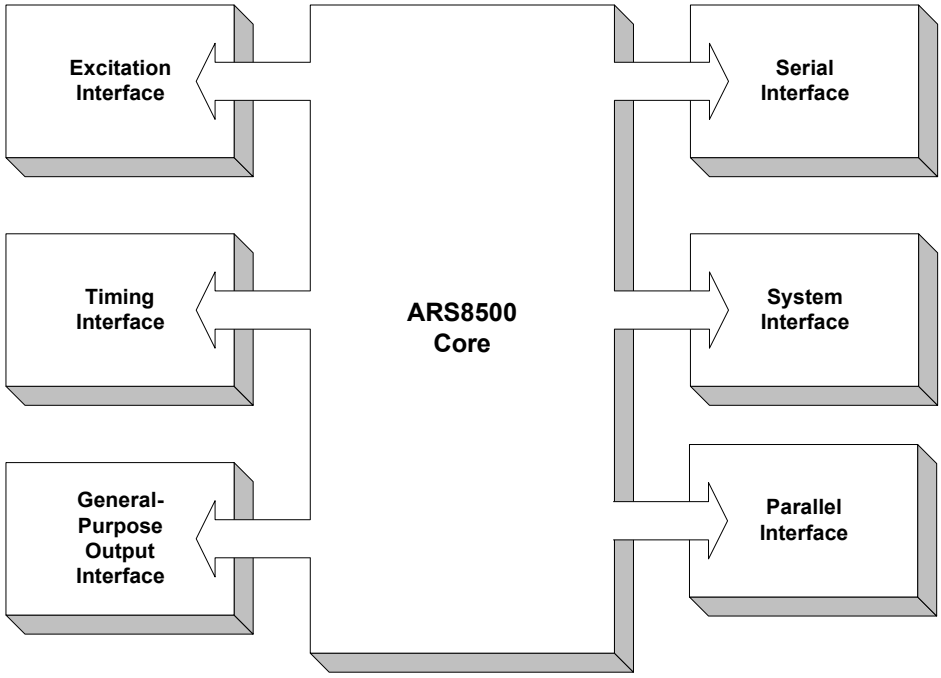
Designers familiar with AuthenTec's AF-S2 sensor will find that the following features are new with the AFS8500:

- Integrated eight-bit parallel bus interface sufficient to support microprocessor requirements…
- Improved ESD Immunity; IEC61000-4-2 Level 4
- Selectable 5Vdc and 3.3Vdc operation.

Module-Level Description

The following diagram shows a high-level view of the AFS8500 sensor and its interface groups.

Figure - Sensor IC Interfaces



The following table provides brief descriptions of each interface.

Table - Sensor IC Interfaces

INTERFACE	DESCRIPTION
Serial	Standard CMOS-level RS-232 NRZ asynchronous serial interface to the AFS8500. Baud rates are pin-selectable up to 921.6Kbaud.
Excitation	Provides interfaces for analog signals requiring off-chip components. These include the PLL charge pump filter and filtering for the finger ring drive signal.
GPO	Four General Purpose Outputs for user notification or device control.
Parallel	This eight-bit parallel interface includes required control signals to communicate directly with many industry-standard microprocessors and busses.

Interface Descriptions

The following table lists the AFS8500 command-byte definitions:

Table: Command-Byte Definitions

COMMAND BYTE	DEFINITION
80h – A4h	Precedes a one-byte AFS8500 register data byte.
A5h - BFh	Reserved.
C0h – C5h	Precedes the 256-pixel data message formatted as six one-bit pixels per byte. The lower three bits indicate the sub-array row.
C6h - CFh	Reserved
D0h – D5h	Precedes the 192-pixel data message formatted as eight one-bit pixels per byte. The lower three bits indicate the sub-array row.
D6h - DDh	Reserved
DEh	Precedes the 16-byte histogram message.
DFh	Precedes the eight-byte Authentication Word
E0h – E5h	Precedes 768-pixel data message formatted as two three-bit pixels per byte. The lower three bits indicate the sub-array row.
E6h –EFh	Reserved
F0h –F5h	Precedes 576-byte pixel data message formatted as eight three-bit pixels per three bytes. The lower three bits indicate the sub-array row.
F6h –FFh	Reserved

Register Data Format

When a request to read registers is received, initiated by a rising edge on the *Read Registers* bit (Bit 1 in Register 81h), all register values are returned, each preceded by the command byte for the register.

The command byte for the first register (80h) is sent first, followed by its data byte. This is followed by the command byte for the second register (81h) and its data byte and so on until finally the last register command is sent, followed by the byte that defines the contents of that register.

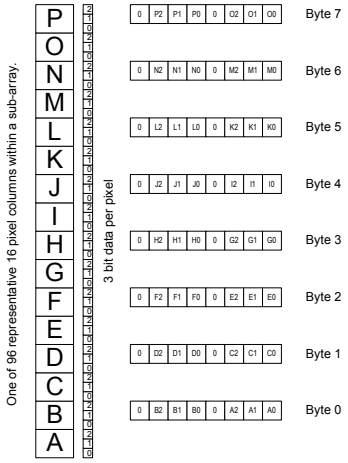
Image Data Formats

While in Measure mode, pixel data for each of the six sub-arrays is returned as it is received. Data for each sub-array is preceded by the command byte for that sub-array as seen in the preceding table, Command-Byte Definitions. The AFS8500 scans by default from the bottom up (the Pin 1 edge) and from the right to the left.

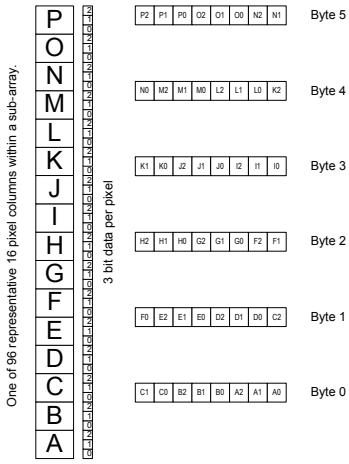
> **Note:** When using AuthenTec's API, all image data formats described in this section are converted to standard eight-bit format.

The AFS8500 is made up of six horizontal sub-arrays numbered 0 through 5. Each sub-array is comprised of 96 columns of 16 pixels. For this discussion, let's assign A through P to the pixels where A is the bottom and P is the top pixel of a representative column of a representative sub-array. Several alternate image data representations can be specified by the *Data Format* bits in Register 97h. Here are these representations in descending order of required bandwidth:

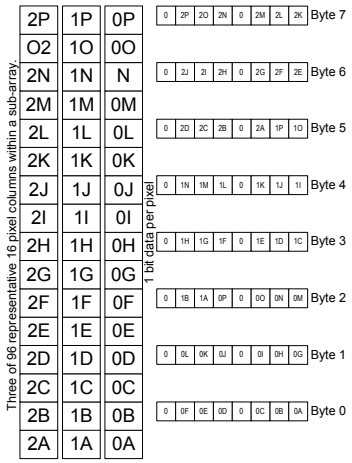
- **Eight bytes per column** – A three-bit pixel has eight levels of gray scale, in which level zero indicates "no ridge" and seven indicates "ridge". Bits three and seven are always zero. The first byte of the column contains the data of the first two pixels arranged as 0BBB0AAA. The last two pixels of this column are represented in the eighth byte as 0PPP0OOO. This default data representation yields 768 bytes of data per sub-array scan.



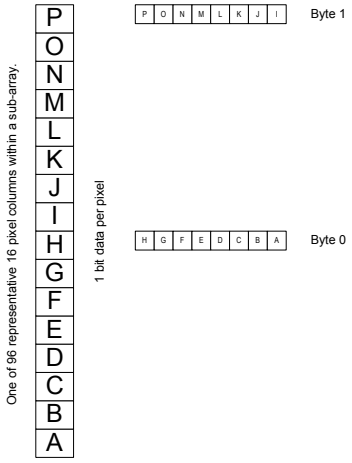
- **Six bytes per column** – A three-bit pixel has eight levels of gray scale, in which level zero indicates "no ridge" and seven indicates "ridge". All bits are used to represent data. The first byte of the column contains the data of the first two pixels plus two bits of the third pixel arranged as CCBBBAAA. This pattern continues such that the sixth byte of the column can be represented as PPPOOONN. This data format yields 576 bytes of data per sub-array scan.



- **Two and two thirds bytes per column** – A one-bit pixel gives a binary representation of the fingerprint image data, in which 0 indicates “no ridge” and 1 indicates “ridge”. Bits three and seven are always zero. Every byte contains the data of six one bit pixels. The first byte of the first column contains the data arranged as 0FED0CBA. The first and second pixels of the second column are combined with the third byte of the first column: 0BAP0ONM. The third byte of the third column completes the pattern with 0PON0MLK. The complete data of three columns is contained in eight bytes of data. An entire sub-array can be represented as 256 bytes of data.



- **Two bytes per column** – A one-bit pixel gives a binary representation of the fingerprint image data, in which 0 indicates “no ridge” and 1 indicates “ridge”. All bits are used to represent data. The first byte of the column contains the data for the first eight pixels arranged as HGFEDCBA and the second byte of the column contains the upper pixels: PONMLKJI. In this format a sub-array contains 192 bytes of data.



After all data for all six sub-arrays is sent, the authentication message is sent, preceded by the command byte for the Authentication Word (DFh). The eight-byte Authentication Word is sent low-order byte first.

The register values are then returned, with each register preceded by the command byte for that register.

Serial Interface

The AFS8500 uses eight-bit data, one start bit, one stop bit, and no parity. The baud rate may be 115.2Kbps, 460.8Kbps, 750.0Kbps, or 921.6Kbps depending on the setting of the BaudSelect pins. See the section on pin descriptions for details.

Communication follows one of four specific protocols. Command bytes are followed by one or more data bytes, described in the section Image Data Formats.

Parallel Interface

The parallel interface is microprocessor bus compatible, and provides a high-speed parallel data and control bus port into the sensor. The interface also provides a selectable interrupt signal (INT) to the processor to signal data availability or it can be used in a polled fashion. The parallel interface uses two I/O ports to minimize resource requirements in the IO port address space of the host architecture.

The system hardware provides an external decode signals (CE#, active low, or CE, active high) to indicate that the address decode is satisfied. The Address/Data port, Address 0, functions like a byte-wide version of the serial interface. The host software writes commands and data or write commands and read streams of parallel data by sending register addresses followed by update values or commands.

With the interrupt enabled, an interrupt is generated on the INT line whenever data from any of the potential data source groups is ready to be read from the sensor. The interrupt goes inactive at the end of each group read. This bus is asynchronous to the internal sensor clock and is synchronized to transitions on the ParRead* and ParWrite* control lines.

The logical model for the two ports is shown in the following table. The parallel interface is comprised of 13 pins: four inputs, eight bi-directional pins, and one output pin. If the parallel interface is not selected, the eight data lines must not be left floating.

At power-up, the interface is in Interrupt Enable mode. The INT pin goes active when the chip has data to transmit. The INT pin stays active until it is explicitly cleared by writing Address 1 with a '1' in the D6 position. If the interrupt is cleared before all the data associated with the interrupt is read, it will not get set again for the remaining bytes. If there is pending data, the interrupt could get set immediately after the last byte of the current message is read.

Table - Parallel Interface I/O Port Assignment

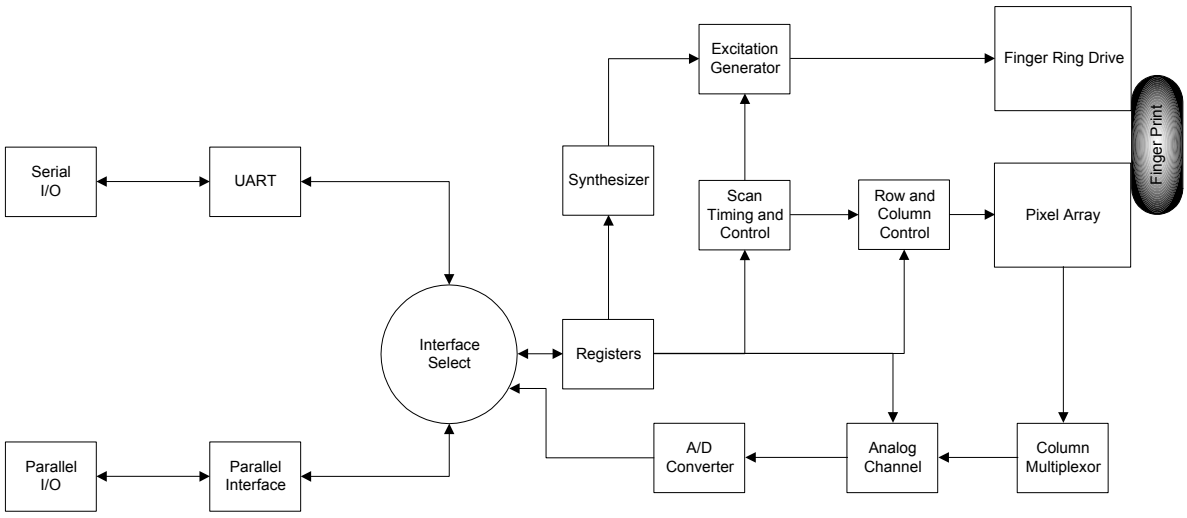
PORT ADDRESS VALUE (SA0)	PORT FUNCTION
0x0	Address/data port
0x1	Control/status port Bit 7- Interrupt Enable/Polled Enable#

	Bit 6- Interrupt Clear Bit 5- 0 Bit 4- 0 Bits [3:1]- Encoded Data Available bits 000-No Data 001-Row Header(one byte) 010-Pixel Data(six or eight bytes) 011-Histogram Data (17 bytes) 100-Authentication Data(nine bytes) 101-Register Data(64 or 74 bytes) Bit 0- Data available handshake bit for Polled operation, active low

Functional Block Diagram

Here is a top-level block diagram of the AFS8500 sensor:

Figure - Sensor IC High Level Block Diagram



Operational Description

Control registers for the sensor are implemented as a master register and a local register. Master registers are written via the selected interface, either serial or parallel. Local registers provide the actual controls and are updated from the master registers before each detection cycle, before an image scan, or via an Ops Reset.

The sensor is in the idle state after a reset. In the idle state, array power is turned off and the sensor checks for a finger present at a rate programmed by the Finger Detect Rate setting (Register 83h). The reset value for this field puts the sensor into Continuous Detection mode, where the Excitation Generator is always on (at a frequency and amplitude determined by the Detect Frequency and Detect Amplitude settings). Other settings result in the Excitation Generator being turned on for 128µs at the programmed rate.

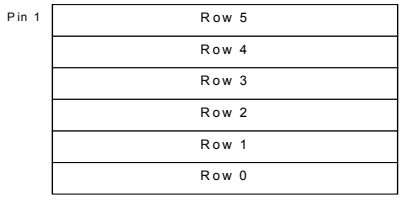
A synchronous phase detector is used to compare the phase of the signal at the finger drive output (FDRV) with an internal reference signal. The internal reference is the excitation generator output with a delay determined by the CALRES (Register 84h) and CALCAP (Register 85h) settings. The phase detector output is used to indicate if a finger is present. It is active when the finger drive signal is delayed by more than the reference signal.

A programmable delay period (set by Debounce Delay in Register 83h) starts when the finger detect output stays active. The delay period is restarted if the finger detect output goes inactive.

After the Debounce Delay time period has elapsed with the finger detect output high, the array power is turned on and the sensor switches to Measure mode. In Measure mode, the frequency and amplitude of the Excitation Generator are determined by the Measure Frequency and Measure Amplitude settings. Also, the finger detection output is considered not valid in Measure mode (since the detection and measurement frequencies can be different) and is not used. A fixed power-up delay of 32.768 ms occurs before the sensor begins imaging.

Before beginning an image scan, the sensor waits for some conditions to be met. The conditions are that no data is being received, that the transmit buffer is empty, and that scanning is enabled (either via the continuous scan bit or a single trigger). When these conditions are met, local registers are updated from master registers and image scanning begins.

Figure - Row Numbering



The array layout and row numbering are shown in the preceding illustration. Each row consists of 96 columns of sixteen pixels, so the complete array has 96 rows x 96 columns. During imaging, the first column (in the bottom right corner as shown in the illustration) is powered up and the signals from each of the pixel amplifiers are demodulated, sampled, digitized and returned to the host computer. Adjacent columns are also powered up depending on the Z-Matrix Horizontal Pattern setting, and pixels in adjacent rows are also powered up using the Z-Matrix Vertical Pattern Setting. Signals from adjacent pixels are summed with the current pixel signal if the Z-Matrix Enable bit is set.

The time to sample and convert one column vector (sixteen pixels) is set by the Column Scan period (Register 88h). Imaging continues across the row until all columns have been sampled. There is an additional column scan time between the last column in a row and the start of the next row.

After the last column in the last row has been sampled, the sensor switches back to detect mode. The finger detector output is ignored for 32µs to allow the Excitation Generator time to switch back to the detect settings for frequency and

amplitude. The finger detector output is then sampled for another 96µs. If the output remains active, another image scan begins (after the conditions ready to being a scan are met).

During this interval, the authentication word (nine bytes including header) and register settings used for that image (64 or 74 bytes) are sent to the host. Since the next image scan does not start until after the transmit buffer is empty, there may be longer than 128µs between image scans if the host is slow to remove data.

If the finger detector output is not active when it is rechecked at the end of a scan, the array is powered down and the sensor reverts back to checking for a finger at the programmed detect rate.

If the conditions to begin a scan are not met within 100 ms, the sensor switches back to detect mode and checks for a finger present. If a finger is present, the timeout will be restarted. If finger is not present, the array will be powered down and the sensor will return to the finger detect state.

The SLEEP* input can be used to place the chip in a low power mode. This disables the internal clock to put all logic in a static, low power state. The control also resets the image control logic so that array power and excitation generator power are turned OFF. Internal control register settings are retained. The SLEEP* input, when inactive, also places the parallel interface (D[7:0]) pins in a high impedance state.

Recommended Operation

This section describes in more detail some of the operating controls of the sensor and provides recommended settings.

General

The Excitation Bias setting in Register 82h sets the bias in the excitation generator amplifiers. Too low a value will cause amplifier roll-off and distortion at higher frequencies. The 5mA setting (010b) has been found to be adequate for all frequencies with V_{CC} at 5Vdc. However, to minimize power consumption the programmer may wish to uses lower settings when possible.

Drive levels (Detect in Register 86h and Measure in Register 89h) below 2Vdc may cause problems with detect and weak images in measurement mode.

Finger Detection

The finger detect threshold is adjusted by changing the calibration resistor (Register 84h) and capacitor (Register 85h) values. A capacitor setting of six counts higher than where the sensor self-triggers is usually adequate to reliably detect the presence of a finger without nuisance false triggers.

Imaging

Sense amp bias (Register 8Ah) sets the bias in the under-pixel amplifiers. Too low a level may cause attenuation at higher frequencies. A value of 5µA generally works well.

Demodulation phase (Register 8Ch and 8Dh) should be adjusted for maximum signal out.

The Analog Channel Bias and S/H Bias (Register 8Fh) should both be set to high if measurement frequencies exceed 250kHz. Setting these bias bits low will conserve power when the measuring frequency is 125kHz.

The Gain values (Register 8Eh) should be adjusted so the output signal is within the A/D range (one to four Vdc when operating with a 5Vdc supply, 0.7 to 2.8 when operating with a 3.3Vdc). The A/D reference high and low values can then be adjusted so that the high is just above the highest signal, and the low is just below the lowest (non-noise) signal value.

The Carrier Null (Register 90h) can be used to shift the output signal down. This is useful if there is a strong signal but a small amount of ridge-to-valley variation.

HARDWARE INTERFACE DETAILS

Pin List – Asynchronous Serial

Pin assignments of the AFS8500 sensor are shown in the following table:

Table - Pin Assignments

Pin	Mnemonic	Pin	Mnemonic	Pin	Mnemonic	Pin	Mnemonic
1	no connect	37	no connect	73	no connect	109	VSS
2	VSSL	38	BaudSelect1	74	no connect	110	VSS
3	VSSL	39	BaudSelect0	75	ChargePump	111	ParA0
4	VSSL	40	VDDL	76	Xout	112	ParWrite*
5	3.3Vsel	41	VSSL	77	Xin	113	ParRead*
6	no connect	42	VDDi	78	VSS	114	ParCE
7	Sleep*	43	VSS	79	VDD	115	ParCE*
8	reserved	44	VSS	80	Ser_Data_Out	116	VDDi
9	reserved	45	VDDi	81	VSSL	117	VSS
10	reserved	46	Out0	82	VSSL	118	VSS
11	no connect	47	Out1	83	VSSL	119	VDDi
12	no connect	48	Out2	84	reserved	120	VSSL
13	no connect	49	Out3	85	reserved	121	reserved
14	reserved	50	VSS	86	reserved	122	reserved
15	reserved	51	VDDi	87	reserved	123	VSS
16	VDD	52	VDDi	88	VSS	124	VSS
17	VDD	53	VDDi	89	VSS	125	VSS
18	DriveRing	54	DriveRing	90	DriveRing	126	DriveRing
19	DriveRing	55	DriveRing	91	DriveRing	127	DriveRing
20	VSS	56	VSS	92	VDD	128	VDDi
21	VSS	57	VSS	93	VDD	129	VDDi
22	FingerPlate	58	Ser_Data_In	94	ParD0	130	VDDi
23	VSS	59	Interrupt	95	ParD1	131	VSS
24	no connect	60	TxEnable	96	ParD2	132	VDD
25	VSS	61	VDDi	97	ParD3	133	reserved
26	no connect	62	VSS	98	VSS	134	VSSL
27	no connect	63	VSS	99	VDD	135	Reset
28	FingerExcite	64	VDDi	100	ParD4	136	Reset*
29	VDD	65	VSSL	101	ParD5	137	VDDi
30	VDDL	66	VSS	102	ParD6	138	VSS
31	VSSL	67	VSSL	103	ParD7	139	VSS
32	VSSL	68	reserved	104	VSS	140	VDDi
33	PLL_Enable*	69	no connect	105	VDD	141	VDD
34	FingerDetect*	70	VSSL	106	FingerDrive	142	VSS
35	no connect	71	reserved	107	VDD	143	reserved
36	no connect	72	reserved	108	no connect	144	no connect

Pin List – 8-bit Parallel

Pin assignments of the AFS8500 sensor are shown in the following table:

Table - Pin Assignments

Pin	Mnemonic	Pin	Mnemonic	Pin	Mnemonic	Pin	Mnemonic
1	no connect	**37**	no connect	**73**	no connect	**109**	VSS
2	VSSL	**38**	BaudSelect1	**74**	no connect	**110**	VSS
3	VSSL	**39**	BaudSelect0	**75**	ChargePump	**111**	ParA0
4	VSSL	**40**	VSSL	**76**	Xout	**112**	ParWrite*
5	3.3Vsel	**41**	VSSL	**77**	Xin	**113**	ParRead*
6	no connect	**42**	VDDi	**78**	VSS	**114**	ParCE
7	Sleep*	**43**	VSS	**79**	VDD	**115**	ParCE*
8	reserved	**44**	VSS	**80**	Ser_Data_Out	**116**	VDDi
9	reserved	**45**	VDDi	**81**	VSSL	**117**	VSS
10	reserved	**46**	Out0	**82**	VSSL	**118**	VSS
11	no connect	**47**	Out1	**83**	VSSL	**119**	VDDi
12	no connect	**48**	Out2	**84**	reserved	**120**	VSSL
13	no connect	**49**	Out3	**85**	reserved	**121**	reserved
14	reserved	**50**	VSS	**86**	reserved	**122**	reserved
15	reserved	**51**	VDDi	**87**	reserved	**123**	VSS
16	VDD	**52**	VDDi	**88**	VSS	**124**	VSS
17	VDD	**53**	VDDi	**89**	VSS	**125**	VSS
18	DriveRing	**54**	DriveRing	**90**	DriveRing	**126**	DriveRing
19	DriveRing	**55**	DriveRing	**91**	DriveRing	**127**	DriveRing
20	VSS	**56**	VSS	**92**	VDD	**128**	VDDi
21	VSS	**57**	VSS	**93**	VDD	**129**	VDDi
22	FingerPlate	**58**	Ser_Data_In	**94**	ParD0	**130**	VDDi
23	VSS	**59**	Interrupt	**95**	ParD1	**131**	VSS
24	no connect	**60**	TxEnable	**96**	ParD2	**132**	VDD
25	VSS	**61**	VDDi	**97**	ParD3	**133**	reserved
26	No connect	**62**	VSS	**98**	VSS	**134**	VSSL
27	no connect	**63**	VSS	**99**	VDD	**135**	Reset
28	FingerExcite	**64**	VDDi	**100**	ParD4	**136**	Reset*
29	VDD	**65**	VSSL	**101**	ParD5	**137**	VDDi
30	VDDL	**66**	VSS	**102**	ParD6	**138**	VSS
31	VSSL	**67**	VSSL	**103**	ParD7	**139**	VSS
32	VSSL	**68**	reserved	**104**	VSS	**140**	VDDi
33	PLL_Enable*	**69**	no connect	**105**	VDD	**141**	VDD
34	FingerDetect*	**70**	VSSL	**106**	FingerDrive	**142**	VSS
35	no connect	**71**	reserved	**107**	VDD	**143**	reserved
36	no connect	**72**	reserved	**108**	no connect	**144**	no connect

Device Level Interface Specifications

System Interface

Table - System Interface Signal Descriptions

Mnemonic	Pin	Pin Type	Driver Type	Freq (MHz)	Description
Xin	77	I	CMOS	12	Input from crystal oscillator or other external clock source.
Xout	76	O	CMOS	12	Output to crystal oscillator.
Sleep*	7	I	CMOS	N/A	When LOW, forces the AFS8500 into a low-power mode. All clocks are disabled.
Reset*	136	I	CMOS	N/A	Active low reset. This pin has an internal pull-up such that a capacitor to ground can be added to implement a POR (Power-On Reset).
Reset	135	I	CMOS	N/A	Active high reset
IO_SEL	40	I	CMOS	N/A	With **IO_SEL** (Pin 40), selects the active interface as follows: 0 Parallel I/O 1 Serial I/O

Serial Interface

Table - Serial Interface Signal Descriptions

Mnemonic	Pin	Pin Type	Drvr Type	Freq (MHz)	Description
BaudSelect1	38	I	CMOS	N/A	With **BaudSelect0** (Pin39), selects MSB for the serial I/O data rate as follows: **(2:1) Rate/Format** 00 115.2Kbps/NRZ 01 460.8Kbps/NRZ 10 750.0 Kbps/NRZ 11 921.6Kbps/NRZ
BaudSelect0	39	I	CMOS	N/A	With **BaudSelect1** (Pin 38), selects the LSB for the serial I/O data rate.
TxEnable	60	I	CMOS	N/A	Enables transmission during serial comm. Must be tied HIGH if parallel comm is selected.
Ser_Data_In	58	I	TTL	2	Serial NRZ data from an external source at the rate selected by the **BaudSelect** pins, 38 and 39.

Mnemonic	Pin	Pin Type	Drvr Type	Freq (MHz)	Description
Ser_Data_Out	80	O	CMOS	2	Serial NRZ output data to an external target at the rate selected by the **BaudSelect** pins, 38 and 39.

Data is formatted using a standard asynchronous protocol. The idle state of the line is HIGH. Each data byte sent is preceded by a LOW start bit and followed by a HIGH stop bit. Each byte is sent LSB first.

Parallel Interface

Table - Parallel Interface Signal Descriptions

Mnemonic	Pin	Pin Type	Drvr Type	Freq (MHz)	Description
ParCE*	115	I	CMOS	8	Parallel I/F chip enable - active LOW.
ParCE	114	I	CMOS	8	Parallel I/F chip enable - active HIGH.
ParRead*	113	I	CMOS	8	Parallel I/F active LOW Read enable.
ParWrite*	112	I	CMOS	8	Parallel I/F active LOW Write enable.
Interrupt	59	O	CMOS	8	Active HIGH interrupt.
PLL_Enable*	33	I	Digital	-	Set HIGH to bypass internal PLL when operating in parallel mode. In serial mode this pin must be tied LOW.
ParD7	103	B	CMOS	8	Parallel data MSB.
ParD6	102	B	CMOS	8	Parallel data bit D6.
ParD5	101	B	CMOS	8	Parallel data bit D5.
ParD4	100	B	CMOS	8	Parallel data bit D6.
ParD3	97	B	CMOS	8	Parallel data bit D3.
ParD2	96	B	CMOS	8	Parallel data bit D2.
ParD1	95	B	CMOS	8	Parallel data bit D1.
ParD0	94	B	CMOS	8	Parallel data LSB
ParA0	111	I	CMOS	8	Parallel address input A0

General Purpose Output Interface

Table - GP Output Interface Signal Descriptions

Mnemonic	Pin	Pin Type	Drvr Type	Freq (MHz)	Description
Out0	46	O	CMOS	N/A	High to turn ON the current source.
Out1	47	O	CMOS	N/A	High to turn ON the current source.
Out2	48	O	CMOS	N/A	High to turn ON the current source.
Out3	49	O	CMOS	N/A	High to turn ON the current source.

The General Purpose Interface outputs are capable of sourcing up to 5mA. They will not sink current.

Analog Interface

Table - Analog Interface Signal Descriptions

MNEMONIC	PIN	PIN TYPE	DRIVER TYPE	FREQ (MHZ)	DESCRIPTION
FingerDetect*	34	O	CMOS	N/A	Goes LOW when a finger is present on the sensor matrix of the AFS8500. Intended to be used to switch power to the array.
FingerDrive	106	O	Analog	2	This signal energizes the Drive Ring through an external filter. This is the "Excitation Generator" output.
FingerExcite	28	O	Analog	2	Connect to **FingerPlate** (Pin 22).
FingerPlate	22	I	Analog	2	Connect to **FingerExcite** (Pin 28).
ChargePump	75	O	Analog	4	Connect an appropriate filter to this pin if the PLL is enabled by Pin 33.
3.3VSel	5	I	CMOS	0	When HIGH, selects 3.3Vdc operation; when LOW, selects 5Vdc operation

Power Interface

Table - Power Interface Signal Descriptions

MNEMONIC	PIN	DESCRIPTION
VDD	16, 17, 29, 79, 92, 93, 99, 105, 107, 132, 141	Power
VSS	20, 21, 23, 25, 43, 44, 50, 56, 57, 62, 63, 66, 78, 88, 89, 98, 104, 109, 110, 117, 118, 123, 124, 125, 131, 138, 139, 142	Ground
VDDi	42, 45, 51, 52, 53, 61, 64, 116, 119, 128, 129, 130, 137, 140	Imaging power (must be same potential as Power during imaging mode)
VDD_unreg	65	Input to 3.3Vdc regulator
VDDL	30,40*,41	Logic signal that must be tied HIGH
VSSL	2, 3, 4, 31,32,65,67,70,81,82,83,120,134	Logic signal that must be tied LOW

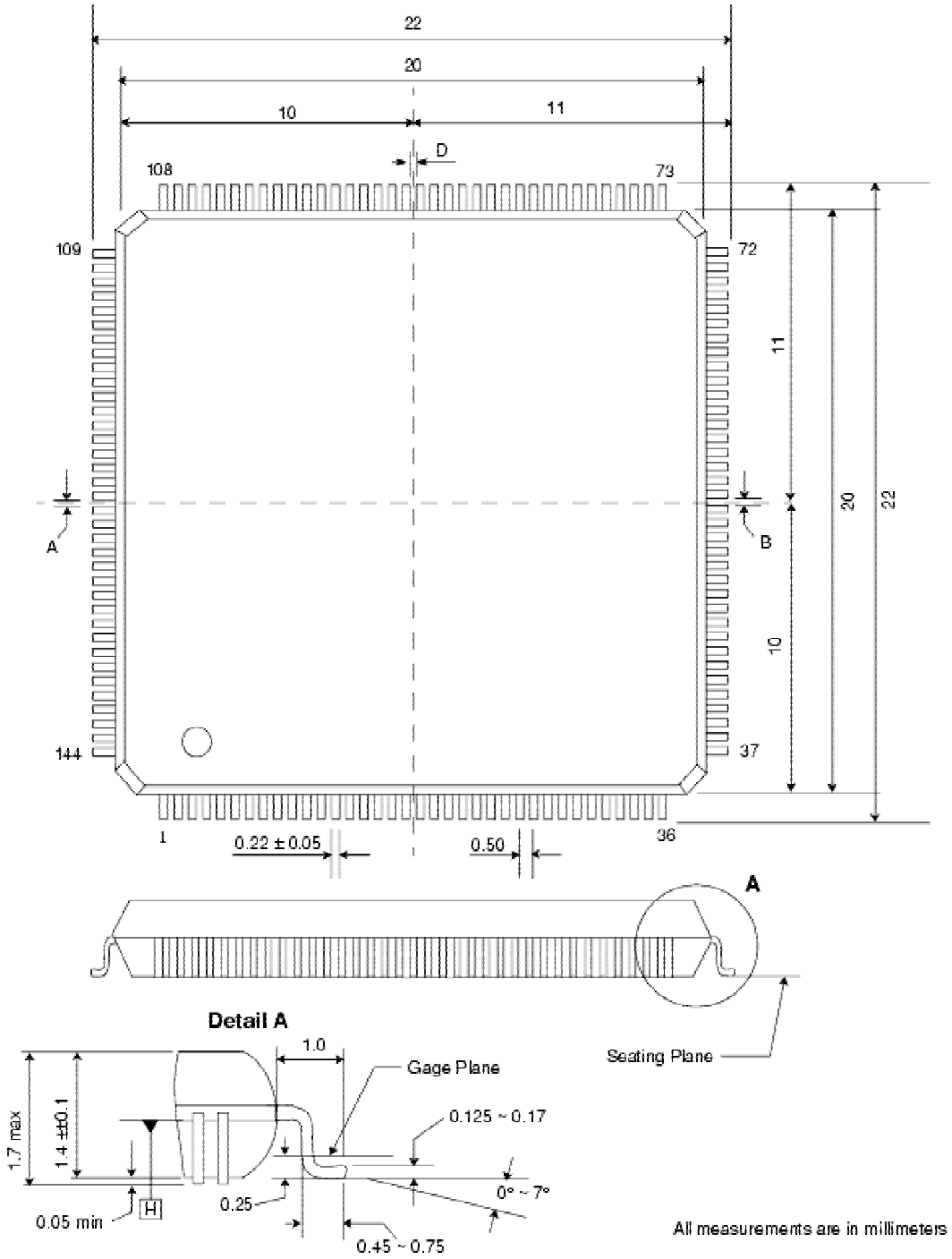
VDDi is turned ON only during imaging. Control for the external power switch is provided by the active LOW **FingerDetect** (Pin 34) output.
Pin 40 changes polarity dependent upon I/F selection.

,

Package

The sensor is packaged in a 144-pin JEDEC-standard LQFP (**L**ow-profile **Q**uad **F**lat **P**ackage) as shown in the following illustration.

Figure - AFS8500 Package Dimensions



Environment

Absolute Maximum Ratings

An absolute maximum rating is the maximum value guaranteed by the ASIC manufacturer. The use of a product in violation of these ratings can result in significant loss of device reliability or even damage to the sensor.

Table - Absolute Maximum Rating

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
VCC	Supply voltage - see Recommended Operating Conditions for effect of 3VOPR control pin	-0.5		5.5	Vdc
VI	Input voltage	-0.5		VCC	Vdc
VO	Output voltage	-0.5		VCC	Vdc
IIK	Input clamp current VI < VSS of VI > VCC			±20	mA
IOK	Output clamp current VO < VSS of VO > VCC			±20	mA
TSTG	Storage temperature	-65°C -85°F		150°C 302°F	
Latch-up	Latch-up immunity	±100			mA

Recommended Operating Conditions

Table - Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
Vcc	Supply voltage - 3VOPR (Pin 5) = 0Vdc	4.0	5.0	5.5	Vdc
Vcc	Supply voltage - 3VOPR = Vcc	3.0	3.3	3.6	Vdc
VI	Input voltage	0		Vcc	Vdc
Vo	Output voltage	0		Vcc	Vdc
VIH	High level input voltage	2.0		Vcc	Vdc
VIL	Low level input voltage	0		1.6	Vdc
tt	Input transition (rise and fall) time	0		3	nSec
Tjr	Junction temperature range (recommended)	-20°C -4°F		45°C 113°F	
Tjm	Junction temperature range (maximum)	-20°C -4°F		85°C 185°F	

Warning

The AFS8500 remains fully operational in junction temperature regimes that are high enough to be potentially uncomfortable for the user.

For reasons of safety and protection, AuthenTec reference designs include circuitry that serves to manage the junction temperature by controlling the supply current. If the hardware developer elects not to use the AuthenTec-provided control circuit design, it will then be essential that an equivalent design be developed and implemented.

DC Electrical Characteristics

Table - DC Electrical Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VOH	High level output voltage	IOH=Rated	Vcc-0.3			Vdc
VOL	Low level output voltage	IOL=Rated			0.3	Vdc
IIL	Low level input current	VI=VIL(min)			±1	µA
IIHI	High level input current	VI=VIH(max)			±1	µA
IOZ	High impedance state output current				±20	µA
Iccq Sleep	Quiescent supply current	VIN=Vcc or VIN=VSS Vcc=Max			20	µA
Iccq Idle	Quiescent supply current	VIN=Vcc or VIN=VSS Vcc=Typ		30		mA
Iccq Imaging	Quiescent supply current	VIN=Vcc or VIN=VSS Vcc=Max		65	80	mA

Power Dissipation

In the quiescent state the sensor draws about 30mA with the supply voltage at 5.0Vdc typical.

In the imaging state, the sensor current depends on the sense amplifier bias and the Z-Matrix kernel (cloud) size

Clock Generation and Distribution

The input clock is 12 MHz, either generated from a crystal using an on-board oscillator or driven from an external source.

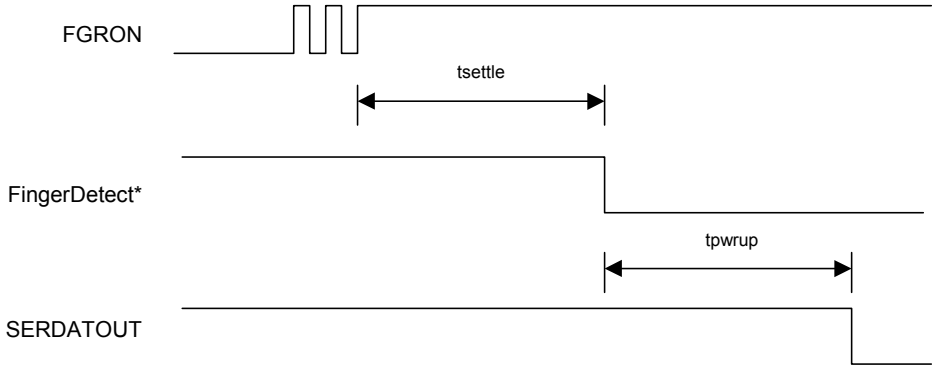
An internal PLL multiplies the input frequency by a factor of four to generate an internal 48MHz clock. All logic runs off the input clock. The serial interface derives baud values from the 48MHz clock.

Timing Diagrams

Image Scan Timing

When a finger is detected, the array is powered up and the sensor begins sending image data. The following diagram shows the timing associated with this process.

Diagram - Image Scan Timing



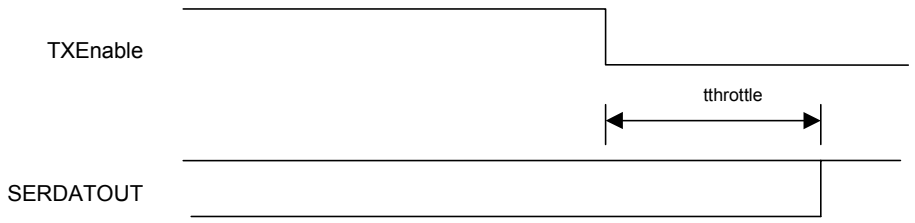
FGRON is the output of the on chip finger detector. Note that the ability to detect a finger is dependent on the **CALCAP**, **CALRES**, **DETDRIVE**, **DETFREQ**, and **EXCITCTRL** register settings. Assuming that these are set correctly, FGRON will go active after a finger is placed on the sensor.

After the FGRON signal has stabilized in the high state, a settling timer (tsettle) is started. The finger settling delay is programmable over the range from 31.25ms to 250ms. The settling delay time is reset if FGRON is ever sampled low. After the settling time, the array power is turned ON and a fixed power-up delay period (tpwrup) of 32.768 ms is started. After the power-up delay, imaging is started (assuming conditions necessary for scanning are met). Image data will begin to be sent one column scan period later.

Serial Interface TXEnable response

The **TXEnable** input (Pin 60) can be used to throttle the data output from the chip. The following diagram shows the timing associated with transmit disabling.

Diagram - TXEnable Response Timing



The serial out circuitry in the sensor consists of a one-byte buffer feeding an output shift register. The **TXEnable** input is sampled whenever the output shift register is empty; the shift register is not loaded until **TXEnable** is active. As long as **TXEnable** is de-asserted more than 35nSec before the end of the stop bit, data transmission will stop at the end of the current byte.

As mentioned earlier, the scan is also paused if the internal buffers are not ready to send data. This feature can be disabled so that column scan timing is not altered and these conditions instead cause loss of image data. The amount of time that **TXEnable** can be de-asserted will then be limited by the column scan period setting and the data removal rate. If **TXEnable** is de-asserted for more than the difference between the two column scan periods and the time to send 16 bytes, image data will be lost.

SLEEP* Response

The SLEEP* input can be used to put the sensor in a low power state. It does this by disabling the internal oscillator and PLL so the clock is not running. After SLEEP* is brought HIGH, an interval of time (initial estimate is 200µs) must be allowed for the oscillator to start up and the PLL to stabilize prior to communicating with the sensor.

Parallel Interface

Write Timing

Data is written to the parallel interface at the rising edge of ParWrite* and both chip select pins (Pin 114 = CE and Pin 115 = CE*) are active. The following diagram shows the timing requirements for Write operations.

Diagram - Parallel Interface Write Timing

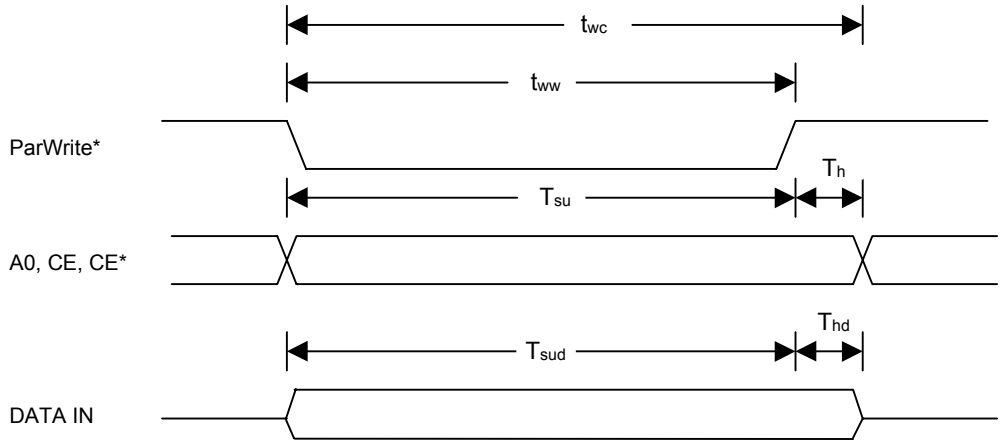


Table - Parallel Interface Write Timing Parameters

PARM	DESCRIPTION	MIN	MAX	UNITS
twc	Write cycle time	80	-	nsec
tww	Write pulse width	50	-	nsec
tsu	Setup time, address or chip select to ParWrite* (Pin 112) rising edge	25	-	nsec
th	Hold time, address or chip select from ParWrite* rising edge	5	-	nsec
tsud	Setup time, data to data to ParWrite* rising edge	25	-	nsec
thd	Hold time, data from ParWrite* rising edge	5	-	nsec

Read Timing

Data is read from the parallel interface when ParRead* is LOW and both chip select pins (Pin 114 = CE and Pin 115 = CE*) are active. The following diagram shows the timing requirements for Read operations.

Diagram - Parallel Interface Read Timing

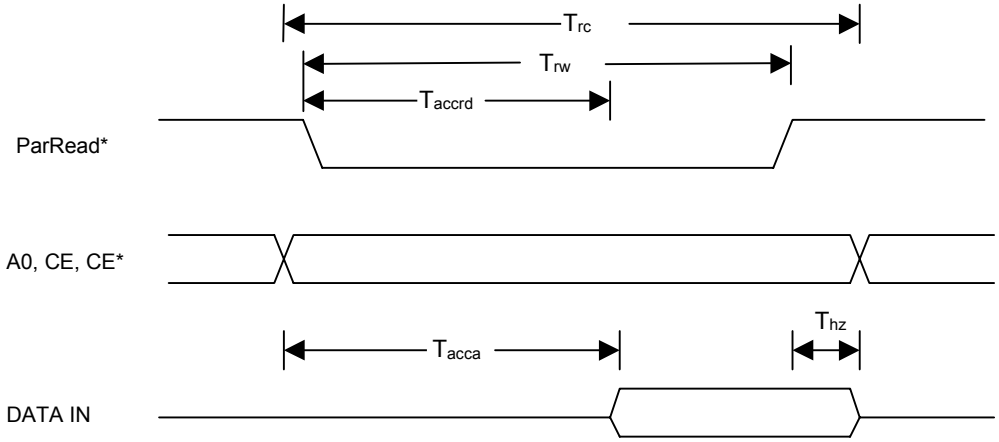


Table - Parallel Interface Read Timing Parameters

PARM	DESCRIPTION	MIN	MAX	UNITS
trc	Read cycle time	80	-	nsec
trw	Read pulse width	50	-	nsec
taccrd	Access time from read low	45	-	nsec
tacca	Access time from address or chip select	55	-	nsec
tbz	Output high impedance from ParRead* (Pin 113) or chip select	5	-	nsec

SOFTWARE INTERFACE DETAILS

Register Map

The following table shows the registers of the AFS8500 and their reset values. Registers that affect imaging are buffered so that they do not change in the middle of a scan. Data is written to the buffer registers using the internal serial interface.

The buffer registers are transferred to output registers at the start of each image scan, or at the start of each detection cycle, or when an "Ops Reset" occurs.

Table - Summary of Data Registers

REG	D6	D5	D4	D3	D2	D1	D0	RESET
	Control #1 (CTRL1)							
80h	Reserved	Reserved	Reserved	Reserved	Register Update	Scan Reset[3]	Master Reset[3]	00h
	Control #2 (CTRL2)							
81h	Reserved	Reserved	Reserved	Disarm Scan Trigger[3]	Arm Scan Trigger[3]	Read Registers[3]	Continuous Scan	00h
	Excitation Common Controls (EXCITCTRL)							
82h	Reserved	Reserved	Reserved	Reserved	Excitation Bias	Excitation Bias	Excitation Bias	02h
	Detect Control (DETCTRL)							
83h	Reserved	Debounce Delay	Debounce Delay	Reserved	Reserved	Detect Rate	Detect Rate	13h
	Calibration Resistor (CALRES)							
84h	Reserved	Reserved	Reserved	Reserved	Cal Resistor	Cal Resistor	Cal Resistor	07h
	Calibration Capacitor (CALCAP)							
85h	Cal Capacitor	Cal Capacitor	Cal Capacitor	Cal Capacitor	Cal Capacitor	Cal Capacitor	Cal Capacitor	7Fh
	Detect Drive (DETDRV)							
86h	Reserved	Reserved	Reserved	Reserved	Reserved	Detect Drive	Detect Drive	02h
	Detect Frequency (DETFREQ)							
87h	Reserved	Reserved	Reserved	Reserved	Detect Freq	Detect Freq	Detect Freq	04h
	Column Scan Time Format (COLSCAN)							
88h	Reserved	Scan Integ Time	Scan Integ Time	Reserved	Col Scan Period	Col Scan Period	Col Scan Period	02h
	Measure Drive (MEASDRV)							
89h	Reserved	Reserved	Reserved	Reserved	Reserved	Measure Drive	Measure Drive	02h
	Measure Frequency (MEASFREQ)							
8Ah	Reserved	Sense Amp Bias	Sense Amp Bias	Reserved	Measure Freq	Measure Freq	Measure Freq	12h
	Z-Matrix Kernel Size (ZMATSIZE)							
8Bh	Reserved	Z-Matrix Vpat	Z-Matrix Vpat	Reserved	Reserved	Z-Matrix Hpat	Z-Matrix Hpat	33h
	Demodulation Phase 2 & 1 (DEMODPHASE 2 & 1							
8Ch	Demod Phase [13]	Demod Phase [12]	Demod Phase [11]	Demod Phase [10]	Demod Phase [9]	Demod Phase [8]	Demod Phase [7]	04h
8Dh	Demod Phase [6]	Demod Phase [5]	Demod Phase [4]	Demod Phase [3]	Demod Phase [2]	Demod Phase [1]	Demod Phase [0]	00h
	Channel Gain (CHANGAIN)							
8Eh	Reserved	Sensor Gain2	Sensor Gain2	Reserved	Reserved	Sensor Gain1	Sensor Gain1	23h
	Imaging Control Register (IMAGCTRLREG)							
8Fh	Reserved	Reserved	Reserved	Z-Matrix Power Enable	Z-Matrix Enable	S/H Bias	Analog Channel Bias	0Fh
	Carrier Null (CARRNULL)							
90h	Reserved	Reserved	Carr Off Null En	Carrier Offset Null	Carrier Offset Null	Carrier Offset Null	Carrier Offset Null	00h

Table - Summary of Data Registers (continued)

REG	D6	D5	D4	D3	D2	D1	D0	RESET
	A/D Reference High (ADREFHI)							
91h	Reserved	Reserved	A/D Ref High	A/D Ref High	A/D Ref High	A/D Ref High	A/D Ref High	14h
	A/D Reference Low (ADREFLO)							
92h	Reserved	Reserved	A/D Ref Low	A/D Ref Low	A/D Ref Low	A/D Ref Low	A/D Ref Low	0Ch
	Start Row (STRTROW)							
93h	Reserved	Reserved	Reserved	Start Row	Start Row	Start Row	Start Row	00h
	End Row (ENDROW)							
94h	Reserved	Reserved	Reserved	End Row	End Row	End Row	End Row	0Fh
	Start Column (STRTCOL)							
95h	Start Column	Start Column	Start Column	Start Column	Start Column	Start Column	Start Column	00h
	End Column (ENDCOL)							
96h	End Column	End Column	End Column	End Column	End Column	End Column	End Column	7Fh
	Data Format (DATAFMT)							
97h	Reserved	Data Format	Data Format	Reserved	Threshold	Threshold	Threshold	04h
	Image Data Control (IMAGCTRL)							
98h	Reserved	Test Register En	Reserved	Histo Full Array	Histo Each Row	Histogram Enable	Imaging Disable	20h
	General Purpose Outputs (GPO)							
99h	Reserved	Reserved	Reserved	GPO3	GPO2	GPO1	GPO0	00h
	Status (STAT)							
9Ah	Reset Occurred[2]	Scan Paused[2]	Framing Error[2]	Scan State[2]	Scan State[2]	Scan State[2]	Scan State[2]	N/A
	Challenge Word 1 (CHWORD1)							
9Bh	Reserved	Reserved	Reserved	Challenge Word [31][1]	Challenge Word [30][1]	Challenge Word [29][1]	Challenge Word [28][1]/ Finger Present[2]	N/A
	Challenge Word 2 (CHWORD2)							
9Ch	Challenge Word [27][1]	Challenge Word [26][1]	Challenge Word [25][1]	Challenge Word [24][1]	Challenge Word [23][1]	Challenge Word [22][1]	Challenge Word [21][1]	00h
	Challenge Word 3 (CHWORD3)							
9Dh	Challenge Word [20][1]/ Sensor Model[2]	Challenge Word [19][1]/ Sensor Model[2]	Challenge Word [18][1]/ Sensor Model[2]	Challenge Word [17][1]/ Sensor Model[2]	Challenge Word [16][1]/ Sensor Model[2]	Challenge Word [15][1]/ Sensor Model[2]	Challenge Word [14][1]/ Sensor Model[2]	31h
	Challenge Word 4 (CHWORD4)							
9Eh	Challenge Word [13][1]/ Sensor Rev[2]	Challenge Word [12][1]/ Sensor Rev[2]	Challenge Word [11][1]/ Sensor Rev[2]	Challenge Word [10][1]/ Sensor Rev[2]	Challenge Word [9][1]/ Sensor Rev[2]	Challenge Word [8][1]/ Sensor Rev[2]	Challenge Word [7][1]/ Sensor Rev[2]	00h
	Challenge Word 5 (CHWORD5)							
9Fh	Challenge Word [6][1]/ Mask Rev[2]	Challenge Word [5][1]/ Mask Rev[2]	Challenge Word [4][1]/ Mask Rev[2]	Challenge Word [3][1]/ Mask Rev[2]	Challenge Word [2][1]/ Mask Rev[2]	Challenge Word [1][1]/ Mask Rev[2]	Challenge Word [0][1]/ Mask Rev[2]	00h
	Reserved Registers							
A0h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A1h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	20h
A2h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A3h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h
A4h	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	00h

Note: 1. Bit is "write-only".
2. Bit is "read-only".
3.

Functional Controls

The following table is an alphabetical listing showing each of the functional controls of the AFS8500, and the mnemonic and hexadecimal number of the registers in which they are located. "Reserved" elements are omitted - see the preceding table for a full listing.

Table - Sensor Functional Controls

CONTROL NAME	REGISTER MNEMONIC	REGISTER NUMBER
A/D Reference High	ADREFHI	91h
A/D Reference Low	ADREFLO	92h
Analog Channel Bias	IMAGCTRLREG	8Fh
Arm Scan Trigger	CTRL2	81h
Calibration Capacitor	CALCAP	85h
Calibration Resistor	CALRES	84h
Carrier Offset Null	CARRNULL	90h
Carrier Offset Null Enable	CARRNULL	90h
Challenge Word	CHWORD1 CHWORD2 CHWORD3 CHWORD4 CHWORD5	9Bh 9Ch 9Dh 9Eh 9Fh
Column Scan Time Format	COLSCAN	88h
Continuous Scan	CTRL2	81h
Data Format	DATAFMT	97h
Debounce Delay	DETCTRL	83h
Demodulation Phase 1	DEMODPHASE1	8Dh
Demodulation Phase 2	DEMODPHASE2	8Ch
Detect Drive	DETDRV	86h
Detect Frequency	DETFREQ	87h
Detect Rate	DETCTRL	83h
Disarm Scan Trigger	CTRL2	81h
End Column	ENDCOL	96h
End Row	ENDROW	94h
Excitation Bias	EXCITCTRL	82h
Framing Error	STAT	9Ah
General Purpose Outputs 0 thru 3	GPO	99h
Image Data Control	IMAGCTRL	98h
Mask Revision	CHWORD5	9Fh
Master Reset	CTRL1	80h
Measure Drive	MEASDRV	89h
Measure Frequency	MEASFREQ	8Ah
Read Registers	CTRL2	81h
Register Update	CTRL1	80h
Reset Occurred	STAT	9Ah
Sample/Hold Bias	IMAGCTRL	8Fh
Scan Paused	STAT	9Ah
Scan Reset	CTRL1	80h
Scan State	STAT	9Ah
Sense Amp Bias	MEASFREQ	8Ah
Sensor Gain 1	CHANGAIN	8Eh
Sensor Gain 2	CHANGAIN	8Eh
Sensor Model	CHWORD3	9Dh

CONTROL NAME	REGISTER MNEMONIC	REGISTER NUMBER
Sensor Revision	CHWORD4	9Eh
Start Column	STRTCOL	95h
Start Row	STRTROW	93h
Threshold	DATAFMT	97h
Z-Matrix Enable	IMAGCTRL	8Fh
Z-Matrix Horizontal Pattern	ZMATSIZE	8Bh
Z-Matrix Power Enable	IMAGCTRL	8Fh
Z-Matrix Vertical Pattern	ZMATSIZE	8Bh

Register Descriptions

The following sections provide complete, bit-by-bit descriptions of each addressable register in the AFS8500 sensor. Following the title of the particular register, its mnemonic identifier is show parenthetically, as is the command value used to address the register (in hexadecimal notation).

For example:

Reset Control (RSTCTRL)

In order to write a register a command byte is sent first, indicating which register is to be updated. The contents of a subsequent data byte is then written to the selected register.

All registers receive their reset value after a Power-On Reset (POR), or after a Master Reset triggered by Bit O of Register 80h. For buffered registers, both the buffer and the output register receive the reset value.

All register bits are read/write unless otherwise indicated. Reserved bits and write-only bits always read back as zero. The individual bits in a register may be written separately, but the entire register must always be read all at once. To read the registers, send a Read Registers request (Bit 1, Register 81h). The AFS8500 responds with 64 bytes, comprised of 32 register address/data pairs.

Control 1 (CTRL1) (80h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Asynch Register Update	Scan Reset	Master Reset
Reset Value	0	0	0	0	0	0	0	0

D6 - D3: Reserved

These bits are not available.

D2: Asynch Register Update

Specify when registers are to be updated.

1 Registers are updated at the same time that they are written.

0 Registers are updated from data written to buffer storage before starting a scan.

D1: Scan Reset

Stop a scan in progress and attempt to detect a finger on the sensor.

If no scan is in progress, no action is taken.

1 Perform a *Scan Reset*.

This bit is self-resetting and will always read back as zero.

D0: Master Reset

Reset all registers and buffers to their initial values.

A *Master Reset* is the same as a Power-On Reset (POR).

1 Perform a *Master Reset*. All registers, including output and buffers are reset to their initial values.

This bit is self-resetting and will always read back as zero.

Control #2 (CTRL2) **(81h)**

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Disarm Scan Trigger	Arm Scan Trigger	Read Registers	Continuous Scan
Reset Value	0	0	0	0	0	0	0	0

D6 - D4: Reserved

These bits are not available.

D3: Disarm Scan Trigger

Disarm a previously-armed Scan Trigger.

1 Disarm the Scan Trigger.

The *Continuous Scan* bit (Bit 0 in this register) must be LOW and a scan must have been previously armed (Bit 2 in this register) for any action to occur.

This bit is self-resetting and will always read back as zero.

D2: Arm Scan Trigger

Make the sensor ready to allow a single image scan.

1 Arm the sensor.

As soon as the necessary conditions are met (that is, finger present, output buffers empty, output channel ready for data, finger settling delay and power up delay expired), an image scan occurs. The *Continuous Scan* bit (Bit 0 in this register) must be LOW for any action to occur.

This bit is self-resetting. This value is read HIGH if a scan is pending, or LOW if one is not. A pending scan can be cleared by a *Scan Reset* (Register 80h, Bit 1) or a *Master Reset* (Register 80h, Bit 0), or by the *Disarm Scan Trigger* bit (Bit 3 in this register).

D1: Read Registers

Read the current state of all of the sensor registers.

1 Read the sensor registers.

This bit is self-resetting and will always read back as zero. The Read Registers request is ignored if the sensor has loopback enabled, or if imaging is in progress.

D0: Continuous Scan

Specify non-stop scanning.

1 Repeated image scans are performed as long as the necessary conditions are met.

0 Controlled scan - single scans are initiated by writing a "1" to the Arm Scan Trigger bit.

Excitation Common Controls (EXCITCTRL) (82h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Excitation Bias Current	Excitation Bias Current	Excitation Bias Current
Reset Value	0	0	0	0	0	0	1	0

D6 - D3: Reserved

These bits are not available.

D2 - D0: Excitation Bias Current

Set finger excitation bias values.

Excitation bias in the AFS8500 sensor are adjustable for the combination of drive ring voltage and drive ring frequency, in both Measurement and Detection modes.

Measurement Mode

Drive Ring Voltage (Measure Drive - Register 89h Bit 0,1)
Drive Ring Frequency (Measure Frequency - Register 8Ah Bit 0,1,2)

Detection Mode

Drive Ring Voltage (Detect Drive - Register 86h Bits 0,1)
Drive Ring Frequency (Detect Frequency - Register 87h Bit 0,1,2)

The following table shows the relationship between drive frequency and drive voltage. Select the appropriate bit setting from this table:

Table – Minimum Excitation Bias Settings for Frequency/Voltage Combinations

FREQUENCY	0.3VDC	1VDC	2VDC	4VDC
125KHz	000	000	000	000
250KHz	000	000	000	001
500KHz	000	000	001	010
1MHz	000	001	010	011
2MHz	001	010	011	100

The bit patterns in the preceding table correspond to excitation bias settings as shown in the following table. Out-of-range settings default to **000.**

BIT SETTING	BIAS CURRENT
000	1.6mA
001	2.8mA
010	5.0mA
011	9.0mA
100	16.5mA

Detect Control (DETCTRL) (83h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	De-bounce Delay	De-bounce Delay	Reserved	Reserved	Detect Rate	Detect Rate
Reset Value	0	0	0	1	0	0	1	1

D6: Reserved

This bit is not available.

D5 - D4: Debounce Delay

Set the delay interval from when a finger is detected on the sensor matrix to when the sensor enters Imaging mode.

It is important to ensure that the finger is firmly placed on the sensor before scanning begins.

Bit Setting	Delay Interval
00	31.25ms
01	62.50ms
10	125.00ms
11	250.00ms

D3 - D2: Reserved

These bits are not available.

D1 - D0: Detect Rate

Set the rate at which the drive ring and the finger detection circuitry are cyclically activated.

The greater the interval in detection cycles, the lower the power consumption by the sensor. For all settings except "continuous", the ON time is 128µs.

Bit Setting	Cyclic Rate
00	Cycles occur every 8.192 ms (122.00 Hz)
01	Cycles occur every 131.072 ms (7.63 Hz)
10	Cycles occur every 1.048 sec (0.95 Hz)
11	Cycles occur continuously

Calibration Resistor (CALRES) (84h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Calibration Resistor	Calibration Resistor	Calibration Resistor
Reset Value	0	0	0	0	0	1	1	1

D6 - D3: Reserved

These bits are not available.

D2 - D0: Calibration Resistor

Select the internal calibration resistance to be used in the finger detection circuit.

The sensor's finger detection filter is an internal R-C network.

BIT SETTING	RESISTANCE VALUE
111	Resistance is 12KΩ
110	Resistance is 10KΩ
101	Resistance is 8KΩ
000	Resistance is 6KΩ

Lower resistance values makes the AFS8500 finger detection circuitry more sensitive. However, false triggering may occur if this value is set too low.

Calibration Capacitor (CALCAP) (85h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Calibration Capacitor	Calibration Capacitor	Calibration Capacitor	Calibration Capacitor	Calibration Capacitor	Calibration Capacitor	Calibration Capacitor
Reset Value	0	1	1	1	1	1	1	1

D6 - D0: Calibration Capacitor

Select the internal calibration capacitance to be used in the finger detection circuit.

The sensor's finger detection filter is an internal R-C network. Using this register, the phase of the calibration signal can be adjusted relative to the signal on the drive ring so that the phase detector that is used to detect a finger is close to the trip point.

BIT SETTING	CAPACITANCE VALUE
0000000	Reference capacitance is 93.75fF
0000001	Reference capacitance is 184.35fF
▼	▼
1111111	Reference capacitance is 11.6pF

Lower capacitance values makes the AFS8500 finger detection circuitry more sensitive, but false triggering may occur if this value is set too low.

Detect Drive (DETDRV) (86h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Reserved	Detect Drive	Detect Drive
Reset Value	0	0	0	0	0	0	1	0

D6 - D2: Reserved

These bits are not available.

D1 - D0: Detect Drive

Set the voltage level of the finger excitation signal generator when in Detection mode.

BIT SETTING	VCC = 5.0VDC	VCC = 3.3VDC
00	0.3 Vpp	0.2 Vpp
01	1.0 Vpp	0.8 Vpp
10	2.0 Vpp	1.8 Vpp
11	4.0 Vpp	2.8 Vpp

Detect Frequency (DETFREQ) (87h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Detect Freq	Detect Freq	Detect Freq
Reset Value	0	0	0	0	0	1	0	0

D6 - D3: Reserved

These bits are not available.

D2 - D0: Detect Frequency

Set the frequency of the finger excitation signal generator when in Detection mode.

Out-of-range values default to the 2.0MHz setting.

BIT VALUE	FREQUENCY
001	125KHz
010	250KHz
011	500KHz
100	1.0MHz
101	2.0MHz

Column Scan Time Format (COLSCAN) (88h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Scan Integration Time	Scan Integration Time	Reserved	Column Scan Period	Column Scan Period	Column Scan Period
Reset Value	0	0	0	0	0	0	1	0

D6: Reserved

This bit is not available.

D5 - D4: Scan Integration Time

Specify the time period available for the operation of the sample/hold circuitry.

BIT SETTING	SCAN INTEGRATION TIME
00	Time is fixed at 28µs. This setting is not valid for a Column Scan Period of 32µs (see the table under *Column Scan Period*, below)
10	Time is fixed at 14µs.
X1	Time is 1/2 the Column Scan Rate as set by Bits 2 - 0.

D3: Reserved

D2 - D0: Column Scan Period

Specify the time period to be used to scan a single column.

Out-of-range settings default to the 2,048µs (**110**) scan period. The time shown in the **Additional Data** column is the time to send the end-of-frame data (a nine-byte authentication word and header plus 64 bytes of register data) and assumes the lowest valid baud.

The data in the **Min Baud** column indicates the lowest baud that can be used in gray-scale mode (non-packed) without causing scanning to pause.

BIT SETTING	COLUMN SCAN PERIOD	IMAGE TIME	ADDITIONAL DATA	FRAME RATE	MIN BAUD
000	32µs	18.6ms	0.365ms	52.7 f/s	none
001	64µs	37.2ms	0.365ms	26.6 f/s	2Mbps
010	128µs	74.4ms	0.792ms	13.3 f/s	921.6Kbps
011	256µs	148.9ms	1.584ms	6.7 f/s	460.8Kbps
100	512µs	297.7ms	1.584ms	3.3 f/s	460.8Kbps
101	1024µs	595.4ms	6.337ms	1.7 f/s	115.2Kbps
110	2048µs	1.19sec	6.337ms	0.8 f/s	115.2Kbps

Measure Drive (MEASDRV) (89h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Reserved	Reserved	Measure Drive	Measure Drive
Reset Value	0	0	0	0	0	0	1	0

D6 - D2: Reserved

These bits are not available.

D1 - D0: Measure Drive

Specify the drive level of the finger excitation signal generator when in Measurement mode.

BIT SETTING	VCC = 5V.0DC	VCC = 3.3VDC
00	0.3 Vpp	0.2 Vpp
01	1.0 Vpp	0.8 Vpp
10	2.0 Vpp	1.8 Vpp
11	4.0 Vpp	2.8 Vpp

Measure Frequency (MEASFREQ) (8Ah)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Sense Amp Bias	Sense Amp Bias	Reserved	Measure Freq	Measure Freq	Measure Freq
Reset Value	0	0	0	1	0	0	1	0

D6: Reserved

This bit is not available.

D5 - D4: Sense Amplifier Bias

Select the bias current for the under-pixel amplifiers.

Each element in the sensor matrix is equipped with an individual amplifier.

Bit Setting	Bias Current
00	2.5µA
01	5µA
10	8µA
11	10µA

D3: Reserved

This bit is not available.

D2 - D0: Measure Frequency

Specify the frequency of the finger excitation signal generator when in Measurement mode.

Out-of-range values default to the 2.0MHz setting.

Bit Setting	Drive Ring Frequency	Min Integration Time (see Reg 88h)
001	125KHz	128µs
010	250KHz	64µs
011	500KHz	32µs
100	1.0MHz	16µs
101	2.0MHz	8µs

Z-Matrix Kernel Size (ZMATSIZE) (8Bh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Z-Matrix Vertical Pattern	Z-Matrix Vertical Pattern	Reserved	Reserved	Z-Matrix Horizontal Pattern	Z-Matrix Horizontal Pattern
Reset Value	0	0	1	1	0	0	1	1

D6: Reserved

This bit is not available.

D5 - D4: Z-Matrix Vertical Pattern

Specify the number of matrix elements, arranged vertically in adjacent sub-array rows, whose under-pixel amplifiers are turned on along with the active pixel column.

This setting defines the vertical dimension of a variable rectangle (the "Z-Matrix" or “cloud” of pixels), centered on the active column, whose horizontal dimension is set by Bits 0 and 1 in this register, the *Z-Matrix Horizontal Pattern*.

Since the fixed vertical dimension of a sub-array row is 16 pixels, this range describes the extent to which the "cloud" overlaps adjacent sub-arrays. For a graphic depiction of this setting, refer to the illustration following the horizontal pattern description.

Bit Setting	Vertical Pixels On
00	±1
01	±2
10	±3
11	±4

D3 - D2: Reserved

These bits are not available.

D1 - D0: Z-Matrix Horizontal Pattern

Specify the number of matrix elements, arranged horizontally in adjacent columns of a sub-array, whose under-pixel amplifiers are turned on along with the amplifiers of the pixels in the active column.

This setting defines the horizontal dimension of a variable rectangle (the "Z-Matrix" or “cloud” of pixels), centered on the active pixel, whose vertical dimension is set by Bits 4 and 5 in this register, the *Z-Matrix Vertical Pattern*.

Bit Setting	Horizontal Pixels On
00	±2
01	±4
10	±6
11	±8

In other words…

00 Sets the range of active elements to be ±2 pixels, for a total width of five pixels:

○●●•●●○

01 Sets the range of active elements to be ±4 pixels, for a total width of nine pixels:

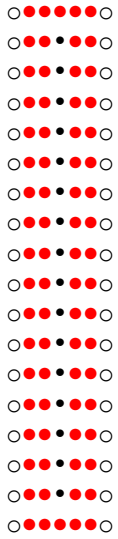
○●●●●•●●●●○

10 Sets the range of active elements to be ±6 pixels, for a total width of 13 pixels:

○●●●●●●•●●●●●●○

11 Sets the range of active elements to be ±8 pixels, for a total width of 17 pixels:

○●●●●●●●●•●●●●●●●●○



During a scan the under-pixel amplifiers of all 16 pixels (•) in a given column are activated at once, as are those of certain adjacent pixels (●) specified by the *Z-Matrix Vertical Pattern* and *Z-Matrix Horizontal Pattern* bits.

The Z-Matrix pattern shown here is the minimum "cloud" (90 pixels) produced by **00** matrix settings – ±1 pixel in the vertical dimension and ±2 pixels in the horizontal. Notice that this vertical setting results in an overlap of one pixel each into the sub-array above and below the currently active one.

Demod Phase 2 (DEMODPHASE2) (8Ch)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Demod Phase [13]	Demod Phase [12]	Demod Phase [11]	Demod Phase [10]	Demod Phase [9]	Demod Phase [8]	Demod Phase [7]
Reset Value	0	0	0	0	0	1	0	0

Demod Phase 1(DEMODPHASE1) (8Dh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Demod Phase [6]	Demod Phase [5]	Demod Phase [4]	Demod Phase [3]	Demod Phase [2]	Demod Phase [1]	Demod Phase [0]
Reset Value	0	0	0	0	0	0	0	0

D13 - D0: Demod Phase 2 and 1

Specify the phase of the demodulation clock relative to the positive zero crossing of the signal on the drive ring.

The bit weighting has the following relative scale:

BIT SETTING	WEIGHT
Bit[13]	Bit Weight = 180 degrees
Bit[12]	Bit Weight = 90 degrees
▼	▼
Bit[0]	Bit Weight = 0.02197256 degrees

For example:

If Bit[13:0] is equal to 3800h, the phase angle is 315 degrees.
If Bit[13:0] is equal to 37FFh, the phase angle is 314.978027344 degrees.

Channel Gain (CHANGAIN) (8Eh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Sensor Gain 2	Sensor Gain 2	Reserved	Reserved	Sensor Gain 1	Sensor Gain 1
Reset Value	0	0	1	0	0	0	1	1

D6: Reserved

This bit is not available.

D5 - D4: Sensor Gain 2

Specify the gain in the second stage of the analog channel.

These bit values produce the multiples shown in the following table:

BIT SETTING	MULTIPLE
00	2x
01	4x
10	8x
11	16

D3 - D2: Reserved

These bits are not available.

D1 - D0: Sensor Gain 1

Specify the gain in the first stage of the analog channel.

These bit values produce the multiples shown in the following table:

BIT SETTING	MULTIPLE
00	2x
01	4x
10	8x
11	16

Imaging Control Register (IMAGCTRL) (8Fh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Z-Matrix Power Mode	Z-Matrix Enable	Sample/Hold Bias	Analog Channel Bias
Reset Value	0	0	0	0	1	1	1	1

D6 - D4: Reserved

These bits are not available.

D3: Z-Matrix Power Mode

Specify power behavior for the Z-Matrix.

BIT SETTING	STATE
1	The Z-Matrix is powered at all times
0	The Z-Matrix is powered only when enabled by Bit 2 of this register

D2: Z-Matrix Enable

Specify adjacent pixel summing.

BIT SETTING	STATE
1	Enable the signals from adjacent pixels to be summed
0	Disable summing from adjacent pixels

D1: Sample/Hold Bias

Specify a bias current setting for the sample/hold circuitry.

BIT SETTING	DESCRIPTION
1	Set standard bias current in the sample/hold amplifier
0	Set sample/hold amplifier bias current to low power mode (valid only if measurement frequency (Register 8Ah) is set to 125KHz)

D0: Analog Channel Bias

Specify a bias current setting for the analog circuitry.

BIT SETTING	DESCRIPTION
1	Set standard current in the analog channel amplifier
0	Set analog bias current to low power mode (valid only if measurement frequency (Register 8Ah) is set to 125KHz)

Carrier Null (CARRNULL) (90h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Carrier Offset Null Enable	Carrier Offset Null	Carrier Offset Null	Carrier Offset Null	Carrier Offset Null
Reset Value	0	0	0	0	0	0	0	0

D6 - D5: Reserved

These bits are not available.

D4: Carrier Offset Null Enable

Specify Carrier Offset Null operation.

BIT SETTING	STATE
1	Enable Carrier Offset Null operation
0	Disable Carrier Offset Null operation

D3 - D0: Carrier Offset Null

Add a negative voltage to the signal prior to the internal analog-to-digital (A/D) conversion of the scanned image.

This table shows the voltages associated with each setting for VCC values of 3.3Vdc and 5.0Vdc. VDAC is the output of the digital-to-analog converter (DAC), and the Output Step Voltage is the voltage summed with the signal.

	3.3VDC		5.0VDC	
VALUE	VDAC	OUTPUT STEP VOLTAGE	VDAC	OUTPUT STEP VOLTAGE
0000	0.16Vdc	-2.51Vdc	0.25Vdc	-3.8Vdc
0001	0.33Vdc	-2.31Vdc	0.5Vdc	-3.5Vdc
0010	.66Vdc	-1.98Vdc	1.0Vdc	-3.0Vdc
▼	▼	▼	▼	▼
1110	2.31Vdc	-0.33Vdc	3.5Vdc	-0.5Vdc
1111	2.64Vdc	0.0Vdc	4.0Vdc	0.0Vdc

A/D Reference High (ADREFHI) (91h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	A/D Ref High	A/D Ref High	A/D Ref High	A/D Ref High	A/D Ref High
Reset Value	0	0	0	1	0	1	0	0

D6 - D5: Reserved

These bits are not available.

D4 - D0: A/D Reference High

Specify the high reference voltage for the sensor's internal analog-to-digital (A/D) converter.

The actual voltage reference to the A/D is 0.15625 * (setting + 1). For example, the reset value of 14h would yield 3.28125Vdc when VCC = 5Vdc, and 2.165625Vdc when VCC = 3.3Vdc.

A/D Reference Low (ADREFLO) (92h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	A/DRef Low	A/D Ref Low	A/D Ref Low	A/D Ref Low	A/D Ref Low
Reset Value	0	0	0	0	1	1	0	0

D6 - D5: Reserved

These bits are not available.

D4 - D0: A/D Reference Low

Specify the low reference voltage for the sensor's internal analog-to-digital (A/D) converter.

The actual voltage reference to the A/D is 0.15625 * (setting + 1). For example, the reset value of 14h would yield 2.03125Vdc when VCC = 5Vdc, and 1.340625Vdc when VCC = 3.3Vdc.

Start Row (STRTROW) (93h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Start Row	Start Row	Start Row	Start Row
Reset Value	0	0	0	0	0	0	0	0

D6 - D4: Reserved

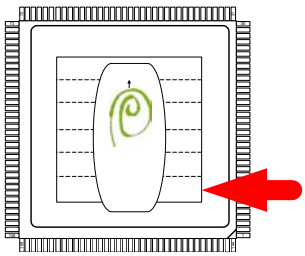
These bits are not available.

D3 - D0: Start Row

Specify the sensor matrix starting row for an image scan.

The default starting row for a complete scan of the entire sensor matrix is Row 0, as shown in the illustration.

- If the starting row set in this register is the same as the ending row set in Register 94h, only that single row will be scanned.
- If the ending row number is lower than the starting row number the scanning process will wrap around to Row 0 after completing Row 5.



Physically, there are only six rows (up to 101b) in the AFS8500 sensor, but this register supports up to sixteen rows for future expansion.

All values greater than 5 set in this register result in the end row = 5.

End Row (ENDROW) (94h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	End Row	End Row	End Row	End Row
Reset Value	0	0	0	0	1	1	1	1

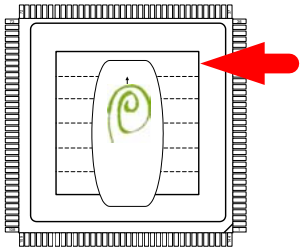
D6 - D4: Reserved

This bit is not available.

D3 - D0: End Row

Specify the sensor matrix ending row for an image scan.

The default ending row for a complete scan of the entire sensor matrix is Row 5, as shown in the illustration.



- If the ending row set in this register is the same as the starting row set in Register 93h, only that single row will be scanned.
- If the ending row number is lower than the starting row number the scanning process will wrap around to Row 0 after completing Row 5.

Physically, there are only six rows (up to 101b) in the AFS8500 sensor, but this register supports up to sixteen rows for future expansion.

Start Column (STRTCOL) (95h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Start Column	Start Column	Start Column	Start Column	Start Column
Reset Value	0	0	0	0	0	0	0	0

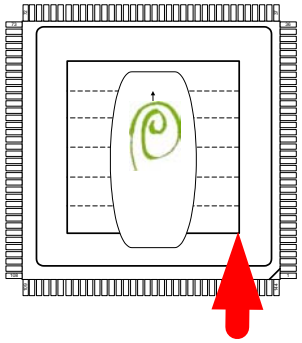
D6 - D5: Reserved

These bits are not available.

D4 - D0: Start Column

Set the sensor matrix starting column for an image scan.

The default starting column for a complete scan is Column 0 in Row 0, as shown in the illustration. A scan may be specified to start at Column 0, 4, 8, 12, … and so on, up to Column 92 (in increments of 4) by writing the column number divided by four into the Start Column register. Each row has 96 columns (numbered 0 through 95).



Values greater than 17h written to the Start Column register result in a scan starting at Column number 92.

End Column (ENDCOL) (96h)

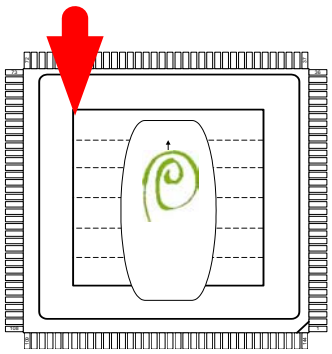
	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	End Column	End Column	End Column	End Column	End Column
Reset Value	0	1	1	1	1	1	1	1

D6 - D5: Reserved

These bits are not available.

D4 - D0: End Column

Specify the sensor matrix ending column for an image scan.



The default ending column for a complete scan of the entire sensor matrix is Column 95 in Row 5, as shown in the illustration. A scan may be specified to end on Column 0, 4, 8, 12 … and so on, up to Column 92 (in increments of 4) by writing the column number divided by four into the End Column register.

Values greater than 17h written to the End Column register result in a scan ending at column number 95.

A scan begins on the column defined by the value of the Start Column register times 4 and ends including the column defined by the value of the End Column register times 4.

The value specified for the End Column register must not be less than the value specified for the Start Column register.

Data Format (DATFMT) (97h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Data Format	Data Format	Reserved	Threshold	Threshold	Threshold
Reset Value	0	0	0	0	0	1	0	0

D6: Reserved

This bit is not available.

D5 - D4: Data Format

Specify the format for image data output.

BIT SETTING	DESCRIPTION
00	Normal operation. Image data is three bits per pixel and packed two pixels per byte. A row is 768 bytes
01	Image data is packed using all eight bits where eight, three-bit pixels are sent as three bytes. Each row contains 576 bytes of data
10	mage data is sent one bit per pixel. Data format is same as normal (only six bits used per byte). Three columns are sent as eight bytes. Each row contains 256 bytes
11	Image data is one bit per pixel and packed eight bits per byte. Three columns are sent as six bytes. Each row contains 192 bytes

D3: Reserved

This bit is not available.

D2 - D0: Threshold

Specify the threshold value for one-bit-per-pixel (packed) mode.

Use these bits for data formats **10** and **11**. In data formats **00** and **01** the settings are ignored.

A pixel with an A/D value greater than or equal to the threshold value is sent as a 1.

Image Data Control (IMAGCTRL) (98h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Test Register Enable	Reserved	Histo Full Array	Histo Each Row	Histo Enable	Imaging Disable
Reset Value	0	0	1	0	0	0	0	0

D6: Reserved

This bit is not available.

D5: Test Register Enable

Specify Test Register operation.

Bit Setting	Description
1	Test Registers (registers with command addresses above 9Fh) are returned with register messages (default)
0	Test registers are not returned

D4: Reserved

This bit is not available.

D3: Histogram Full Array

Specify histogram size.

Bit Setting	Description
1	Take histogram data over the full image array set by the starting column (Register 95h) and ending column (Register 96h)
0	Take histogram data only from those of the center 64 x 64 pixels that are included in the scan size defined by the starting column (Register 95h) and ending column (Register 96h) (default)

D2: Histogram Each Row

Specify the method of histogram data transmission.

Bit Setting	Description
1	Send histogram data at the end of each row
0	Send histogram data after the image scan is complete (default)

D1: Histogramming Enable

Specify histogram operation.

BIT SETTING	DESCRIPTION
1	Enable histogramming
0	Do not enable histogramming (default)

D0: Imaging Disable

Specify "histogram-only" operation.

BIT SETTING	DESCRIPTION
1	Image data and the Authentication Word are not returned when imaging. This setting greatly reduces bandwidth
0	Image data and the Authentication Word are returned when imaging

General Purpose Outputs (GPO) (99h)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	GPO3	GPO 2	GPO 1	GPO0
Reset Value	0	0	0	0	0	0	0	0

The General Purpose Output pins are open drain. They can source up to 2mA.

D6 - D4: Reserved

These bits are not available.

D3: GPO3

Specify operation of General Purpose Output 3.

Bit Setting	State
1	Turn GPO3 ON
0	Turn GPO3 OFF

D2: GPO2

Specify operation of General Purpose Output 2.

Bit Setting	State
1	Turn GPO2 ON
0	Turn GPO2 OFF

D1: GPO1

Specify operation of General Purpose Output 1.

Bit Setting	State
1	Turn GPO1 ON
0	Turn GPO1 OFF

D0: GPO0

Specify operation of General Purpose Output 0.

Bit Setting	State
1	Turn GPO0 ON
0	Turn GPO0 OFF

Status (STAT) **(9Ah)**

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reset Occured	Scan Paused	Framing Error	Scan State	Scan State	Scan State	Scan State
Reset Value	0	0	0	0	0	0	0	0

All bits in this register are read-only, and are cleared after the register is read.

D6: Reset Occurred

If this bit is HIGH, a Master Reset input has been asserted.

D5: Scan Paused

If this bit is HIGH, the image scan was paused because the input buffer was full and therefore unable to accept A/D data.

This bit is cleared after the register is read. It is also set during histogram data transmission because the column scan clock is held OFF to allow the histogram data transactions to complete.

D4: Framing Error

If this bit is HIGH, a Serial Interface Framing Error (Stop Bit was not logic 1) occurred since the last time the registers were read.

D3 - D0: Scan State

Read these bits to determine various sensor states.

BIT SETTING	SENSOR STATE
0000	Waiting for a finger to be placed on the detection matrix
0001	In Finger Settling Delay period
0011	In Power-Up Delay period
0100	Z-Matrix is being pre-loaded
0101	Setup for column load
0110	Pre-loading column
0111	Waiting for scan clock
1000	Waiting for row end
1001	Setting up for next row
1010	Post image delay (up to 128µs)
1011	Waiting for Data Send Complete
1100	Waiting to detect finger (128µs)

Challenge Word 1 (CHWORD1) (9Bh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Reserved	Reserved	Reserved	Challenge Word [31]	Challenge Word [30]	Challenge Word [29]	Challenge Word [28] / Finger Present
Reset Value	0	0	0	0	0	0	0	0

D6 - D4: Reserved

WRITE

D3 - D0: Challenge Word [31:28]

Write to this register to alter bits 31 through 28 of the Challenge Word.

READ

D0: Finger Present

Read this register to determine the state of the finger detector after the noise filter.

The value shown presumes that the finger detector has been calibrated.

BIT SETTING	STATE
1	A finger is present on the sensor detection surface
0	No finger is present

Challenge Word 2 (CHWORD2) (9Ch)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Challenge Word [27]	Challenge Word [26]	Challenge Word [25]	Challenge Word [24]	Challenge Word [23]	Challenge Word [22]	Challenge Word [21]
Reset Value	0	0	0	0	0	0	0	0

All bits in this register are write-only. If read, the values are treated as "Don't Cares".

D6 - D0: Challenge Word [27:21]

Write to this register to alter Bits 27 through 21 of the Challenge Word.

Challenge Word 3 (CHWORD3) (9Dh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Challenge Word[20] or Sensor Model	Challenge Word[19] or Sensor Model	Challenge Word[18] or Sensor Model	Challenge Word[17] or Sensor Model	Challenge Word[16] or Sensor Model	Challenge Word[15] or Sensor Model	Challenge Word[14] or Sensor Model
Reset Value	0	0	1	1	0	0	0	1

WRITE…

D6 - D0: Challenge Word [20:14]

Write to this register to alter Bits 20 through 14 of the Challenge Word.

READ…

D6 - D0: Sensor Model [6:0]

Read this register to determine the model number of the sensor.

31h AFS8500, 96 x 96 array.

Challenge Word 4 (CHWORD4) (9Eh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Challenge Word[13] or Sensor Rev	Challenge Word[12] or Sensor Rev	Challenge Word[11] or Sensor Rev	Challenge Word[10] or Sensor Rev	Challenge Word[9] or Sensor Rev	Challenge Word[8] or Sensor Rev	Challenge Word[7] or Sensor Rev
Reset Value	0	0	0	0	0	0	0	0

WRITE…

D6 - D0: Challenge Word [13:7]

Write to this register to alter Bits 13 through 7 of the Challenge Word.

READ…

D6 - D0: Sensor Revision [6:0]

Read this register to determine the revision level of the silicon layers of the sensor.

Challenge Word 5 (CHWORD5) (9Fh)

	D7	D6	D5	D4	D3	D2	D1	D0
	0	Challenge Word[6] or Mask Rev	Challenge Word[5] or Mask Rev	Challenge Word[4] or Mask Rev	Challenge Word[3] or Mask Rev	Challenge Word[2] or Mask Rev	Challenge Word[1] or Mask Rev	Challenge Word[0] or Mask Rev
Reset Value	0	0	0	0	0	0	0	0

WRITE…

D6 - D0: Challenge Word [6:0]

Write to this register to alter Bits 6 through 0 of the Challenge Word.

READ…

D6 - D0: Mask Revision [6:0]

Read this register to determine the revision level of the metal layers of the sensor.

Test Registers (TESTREG 0 – 4) (A0 – A4)

These registers are reserved for factory use.

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