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MBF310

Solid State Fingerprint Sweep Sensor™

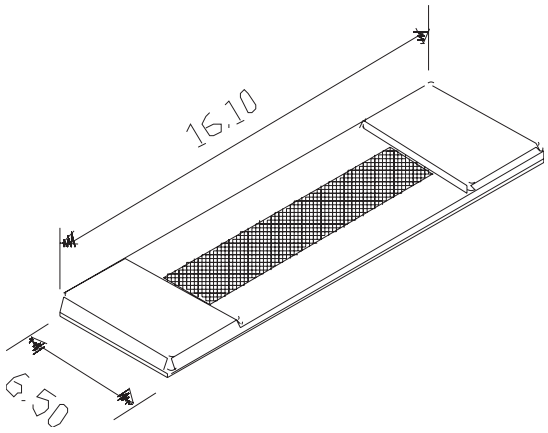
Overview

The Fujitsu MBF310 Solid-State Fingerprint Sweep Sensor is a direct contact, fingerprint acquisition device. It is a high performance, low power, low cost, capacitive sensor composed of a two-dimensional array of metal electrodes in the sensing array. Each metal electrode acts as one plate of a capacitor and the contacting finger acts as the second plate. A passivation layer on the device surface forms the dielectric between these two plates. Ridges and valleys on the finger yield varying capacitor values across the array, and the resulting varying discharge voltages are read to form an image of the fingerprint.

The MBF310 sensor when combined with Sweep Sensor image capture software works by sliding your finger over the sensor surface. Rapid image capture software detects muliple fingerprint images and reconstructs the fingerprint minutia template.

The MBF310 is manufactured in standard CMOS technology. The 218 X 8 sensor array has a 50 µm pitch and yields a 500-dpi image. The sensor surface is protected by a patented, ultra-hard, abrasion and chemical resistant coating.

Package



Features

- Capacitive solid-state device
- 500-dpi resolution (50 µm pitch)
- 1.09 cm x 0.05 cm sensing area
- 218 x 8 sensor array
- 2.7V to 3.3V operating range
- Exceptionally hard protective coating
- Integrated 8-bit analog to digital converter
- One of two bus interfaces:
  8-bit microprocessor bus interface
  Integrated Serial Peripheral Interface
- 2K bytes FIFO
- Auto-finger detection, VitualTouch
- Standard CMOS technology
- Low power, less than 50 mW operating at 3.3V

Applications

- Secure access for databases, networks, local storage
- Portable fingerprint acquisition
- Smart Cards
- Identity verification for ATM transactions
- Cellular phone-based security access
- Access control and monitoring (home, auto, office, etc.)

Table of Contents

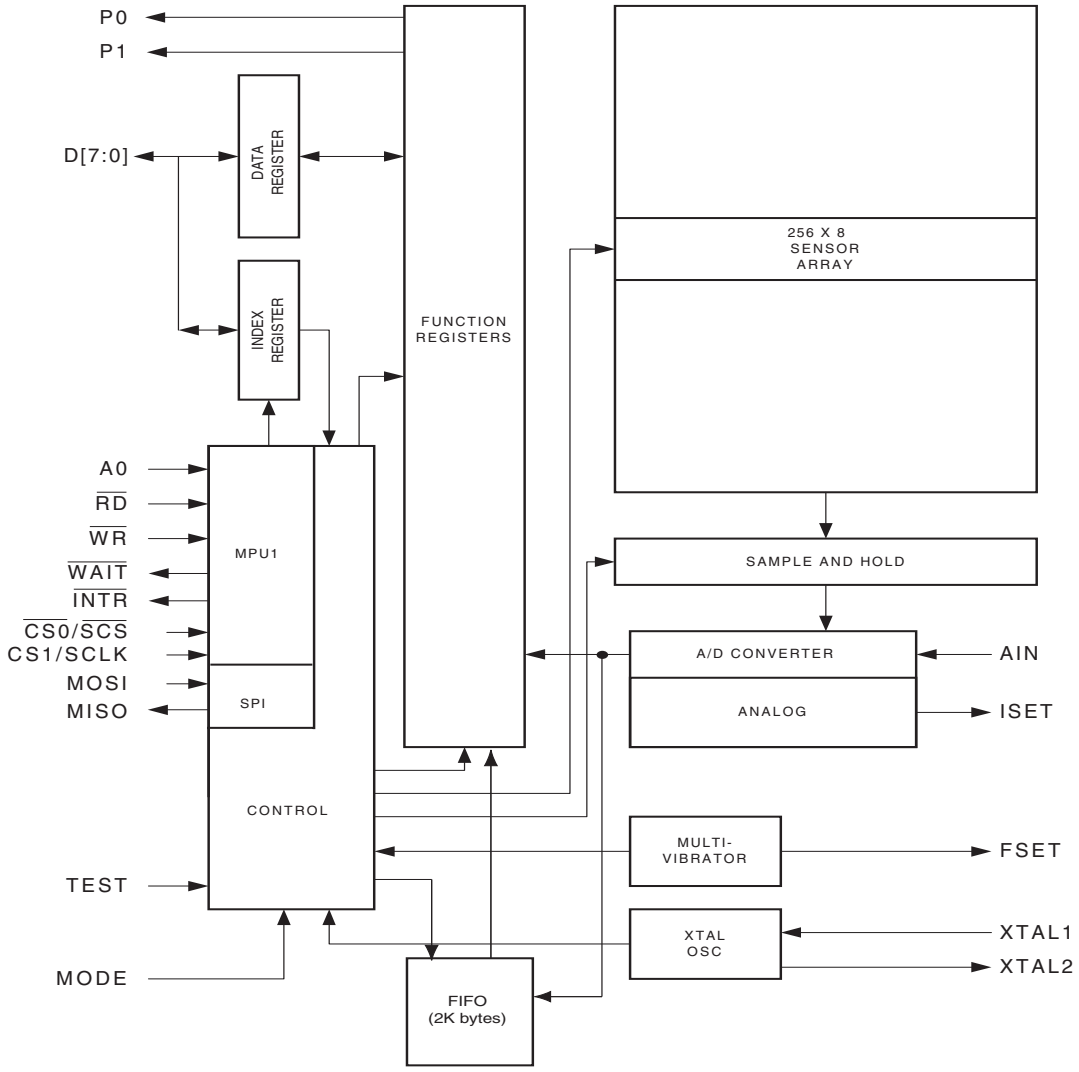
Chip Operation

The sensor array includes 218 columns and 8 rows of sensor plates. Associated with each column are two sample-and-hold circuits. A fingerprint image is sensed or captured one row at a time. This "row capture" occurs in two phases. In the first phase, the sensor plates of the selected row are pre-charged to the VDD voltage. During this pre-charge period, an internal signal enables the first set of sample-and-hold circuits to store the pre-charged plate voltages of the row.

In the second phase, the row of sensor plates is discharged with a current source. The rate at which a cell is discharged is proportional to the "discharge current." After a period of time (referred to as the "discharge time"), an internal signal enables the second set of sample-and-hold circuits to store the final plate voltages. The difference between the precharged and discharged plate voltages is a measure of the capacitance of a sensor cell. After the row capture, the cells within the row are ready to be digitized.

The sensitivity of the chip is adjusted by changing the discharge current and discharge time. The nominal value of the current source is controlled by an external resistor connected between the ISET pin and ground. The current source is controlled from the Discharge Current Register (DCR). The discharge time is controlled by the Discharge Time Register (DTR).

Block Diagram



Connection Diagram

Ball No.	Ball I/O Function
N4	CVDD1
G4	CVSS1
A4	CS1 / SCLK
P4	$\overline{\text{CSO}}$ / $\overline{\text{SCS}}$
H4	A0
B4	$\overline{\text{RD}}$
R4	$\overline{\text{WR}}$
J4	D0
C4	D1
S4	D2
K4	D3
D4	RVDD1
T4	RVSS1
L4	D4
E4	D5
U4	D6
M4	D7
F4	$\overline{\text{WAIT}}$
V4	$\overline{\text{INTR}}$

V3	RVDD2
F3	RVSS2
M3	XTAL1
U3	XTAL2
E3	CVDD2
L3	CVSS2
T3	MODE
D3	P0
K3	P1
S3	TEST
C3	MISO
J3	MOSI
R3	RVSS3
B3	TTOUCH
H3	FSET
P3	AIN
A3	ISET
G3	VDDA1
N3	VSSA1

NOTE: Ball I/O Reference page 32 (Physical Dimension Drawing)

NC: No Connection

A1	NC
A6	NC
B1	NC
V1	NC
V6	NC

Pin List

Ball Number	Name	Type	IOL (3.3 V)	IOH (3.3 V)	Description
N4	CVDD1	PWD			Digital Power
G4	CVSS1	GND			Digital Ground
A4	CS1/SCLK	I			Chip Select, Active High
P4	$\overline{CS0}/\overline{SCS}$	I			Chip Select, Active Low
H4	A0	I			Address Input
B4	$\overline{RD}$	I			Read Enable, Active Low
R4	$\overline{WR}$	I			Write Enable, Active Low
J4	D0	I/O	12mA	12mA	Data Bit 0
C4	D1	I/O	12mA	12mA	Data Bit 1
S4	D2	I/O	12mA	12mA	Data Bit 2
K4	D3	I/O	12mA	12mA	Data Bit 3
D4	RVDD1	PWR			I/O Port Power Supply
T4	RVSS1	GND			I/O Port Ground
L4	D4	I/O	12mA	12mA	Data Bit 4
E4	D5	I/O	12mA	12mA	Data Bit 5
U4	D6	I/O	12mA	12mA	Data Bit 6
M4	D7	I/O	12mA	12mA	Data Bit 7
F4	$\overline{WAIT}$	O	8mA	8mA	Wait, Active Low
V4	$\overline{INTR}$	O	8mA	8mA	Interrupt Output, Active Low
V3	RVDD2	PWR			I/O Port Power Supply
F3	RVSS2	PWR			I/O Port Ground
M3	XTAL1	I			Internal Oscillator Input
U3	XTAL2	O			Internal Oscillator Output
E3	CVDD2	PWR			Digital Power Supply
L3	CVSS2	GND			Digital Ground
T3	MODE	I			Mode Select
D3	P0	O	8mA	8mA	Output Port 0
K3	P1	O	8mA	8mA	Output Port 1
S3	TEST	I			Test Mode Enable
C3	MISO	O	8mA	8mA	SPI Output
J3	MOSI	I			SPI Input
R3	RVSS3	GND			Analog Ground
B3	TTOUCH	I			TBD
H3	FSET	O			Sets Internal Multi-vibrator Frequency
P3	AIN	I			Analog Input
A3	ISET	O			Sets Reference Current
G3	VDDA1	PWR			Analog Power Supply
N3	VSSA1	GND			Analog Ground

Pin Descriptions

VDDA1
Power Supply to the analog section of the sensor.

VSSA1
Ground for the analog section of the sensor.

CVDD1, CVDD2, RVDD1, RVDD2
Power supply to the digital logic and I/O drivers. CVDD1 and CVDD2 power the core digital logic, oscillators, and digital inputs. RVDD1 and RVDD2 supply power to the digital output circuits.

CVSS1, CVSS2, RVSS1, RVSS2, RVSS3
Ground for the digital logic and I/O drivers.

CVSS1 and CVSS2 are the ground connections for the core digital logic, oscillators, and digital inputs. RVSS1 and RVSS2 are the ground connections for the digital outputs.

ISET
Connect a 200k ohm resistor between ISET and analog ground VSSA1 to set the internal reference current. The discharge current is a scalar function of the internal reference current.

AIN
Alternate analog input to the A/D converter. Set the AINSEL bit in register CTRLA to select AIN as the input to the A/D converter. Pull this pin to ground, preferably with a resistor.

FSET
Connect a resistor between FSET and ground to set the internal multi-vibrator and automatic finger detection frequency. Use a 56k ohm resistor for standard 12 MHz (±20%) multi-vibrator operation and 1KHz (±20%) automatic finger detection sampling rate.

XTAL1
Input to the internal oscillator. To use the internal oscillator, connect a crystal circuit to this pin. If an external oscillator is used, connect its output to this pin.

XTAL2
Output from the internal oscillator. To use the internal oscillator, connect a crystal circuit to this pin. If an external oscillator is used, leave this pin unconnected.

D[7:0]
Bi-directional data bus. These pins may be left unconnected in SPI mode.

A0
Address input. Drive A0 low to select the address index register. Drive A0 high to select the data buffer. This pin should be connected to ground SPI mode.

$\overline{RD}$

Read enable, active low. To read from the chip, drive $\overline{RD}$ low while $\overline{WR}$ is high and the chip is selected. $\overline{RD}$ has an internal, weak pull-up resistor and may be left unconnected in SPI.

$\overline{WR}$

Write enable, active low. To write to the chip, drive $\overline{WR}$ low while $\overline{RD}$ is high and the chip is selected. $\overline{WR}$ has an internal, weak pull-up resistor and may be left unconnected in SPI.

$\overline{CS0}$ / $\overline{SCS}$

Chip select, active low. The $\overline{CS0}$/$\overline{SCS}$ pin has an internal, weak pull-up resistor. The function of the $\overline{CS0}$/$\overline{SCS}$ pin depends on the MODE pin.

MODE = 0 (Microprocessor Bus Interface Mode)
$\overline{CS0}$/$\overline{SCS}$ functions as an active-low chip select input. Drive $\overline{CS0}$/$\overline{SCS}$ low while CS1 is high to select the chip.

MODE = 1 (SPI Slave Mode)
$\overline{CS0}$/$\overline{SCS}$ functions as an active-low slave chip select input.

CS1 / SCLK

Chip select, active high. The function of this pin depends on the MODE pins.

MODE = 0 (Microprocessor Bus Interface Mode)
CS1/SCLK functions as an active-high chip select input. Drive CS1/SCLK high while CS0-/CSC- is low to select the chip.

MODE = 1 (SPI Slave Mode)
CS1/SCLK functions as the slave serial clock input.

$\overline{INTR}$

Interrupt output, active low. $\overline{INTR}$ is high impedance when it is not active and is driven low when an enabled interrupt event occurs. $\overline{INTR}$ can be enabled if the sensor is in MCU or SPI mode. Connect a pull-up resistor between MISO and VDD to pull-up $\overline{INTR}$ high when idle.

$\overline{WAIT}$

Wait output, active low. $\overline{WAIT}$ is driven low when active and driven high when not active. $\overline{WAIT}$ goes low if the A/D converter is read while an A/D conversion is in progress, or FIFO is empty if A/D converter is read while FIFO is enabled. $\overline{WAIT}$ will remain low until the A/D conversion is completed.

MOSI

SPI Master Output/Slave input. MOSI may be left unconnected in MCU mode. The function of this pin depends on the MODE pin.

MODE = 0 (Microprocessor Bus Interface Mode)
MOSI has no function.

MODE = 1 (SPI Slave Mode)
MOSI functions as the slave serial input.

MISO

SPI Master Input/Slave Output. MISO may be left unconnected in MCU mode. The function of this pin depends on the MODE pin.

MODE = 0 (Microprocessor Bus Interface Mode)
MISO has no function.

MODE = 1 (SPI Slave Mode)
MISO functions as the slave serial data output. Unlike standard SPI, the MISO connection is actively driven high and low when transmitting data and is high impedance when idle. Connect a pull-up resistor between MISO and VDD to pull MISO high when idle.

P0
Port Output 0. This output is controlled by bit 0 of the CTRLC register.

P1
Port Output 1. This output is controlled by bit 1 of the CTRLC register.

MODE
Mode Select pins. MODE select one of two operating modes.

MODE	Description
0	Microprocessor Bus Mode
1	SPI Bus Mode

TEST
Test Mode Enable. It is intended for factory use only.

Device Bus Operation

Microprocessor Bus Interface

The microprocessor bus interface mode uses the following pins: D[7:0], A0, $\overline{RD}$, $\overline{WR}$, $\overline{CS0}$, CS1, $\overline{INTR}$, and $\overline{WAIT}$. Either the internal multi-vibrator or the XTAL1/XTAL2 oscillator can be selected to provide the clock to the chip. The SPI is disabled.

The fingerprint sensor chip uses an indexed addressing scheme to access its function registers. The chip has eight data lines (D[7:0]) and one address line (A0). The address line selects between the index register and the data register. Drive A0 low to select the index register. Drive A0 high to access the function register selected by the index register. The index register retains its value until it is rewritten or the chip is reset.

The chip has four control inputs: $\overline{CS0}$, CS1, $\overline{RD}$, and $\overline{WR}$. Drive $\overline{CS0}$ low and CS1 high to select the chip. Data is latched on the rising edge of WR-.

The chip has two status lines: $\overline{INTR}$ and $\overline{WAIT}$. The $\overline{INTR}$ signal is asserted when an interrupt event occurs. The $\overline{WAIT}$ signal goes low when the A/D converter is read while an A/D conversion is in progress. The $\overline{WAIT}$ signal will be driven high when the A/D conversion is completed. The $\overline{INTR}$ output is high impedance when they are not active. As a result, $\overline{INTR}$ can be active-low WIRE-ORed in conjunction with other interrupts signals.

The SPI interface is disabled when the microprocessor bus interface is selected. A truth table for the microprocessor bus interface is shown below:

Truth Table for the Microprocessor Bus Interface

$\overline{CS0}$	CS1	A0	$\overline{RD}$	$\overline{WR}$	Mode	Data Lines
H	X	X	X	X	De-selected	High Impedance
X	L	X	X	X	De-selected	High Impedance
L	H	X	H	H	Standby	High Impedance
L	H	L	L	H	Read Index Register	Output
L	H	L	H	L	Write Index Register	Input
L	H	H	L	H	Read Data Register	Output
L	H	H	H	L	Write Data Register	Input

Serial Peripheral Bus Interface (SPI) Slave

SPI Bus Mode

SPI (Slave) bus mode uses the following pins: SCLK, $\overline{SCS}$, MOSI, and MISO. Either the internal multivibrator or the XTAL1/XTAL2 oscillator can be selected to provide the clock to the chip. The microprocessor bus is disabled.

SPI Slave Mode

In SPI Slave Mode, the sensor can operate in either SPI mode (0, 0) where CPOL = 0 and CPHA = 0 or SPI mode (1, 1) where CPOL = 1 and CPHA = 1. The SPI Master may clock in commands and clock out data up to 20 Mbits per second. The SPI Master can write and read the registers of the sensor even when the internal multivibrator or XTAL1/XTAL2 oscillator is halted.

- MOSI bits are sampled on the rising edge of SCK
- MISO bits change on the falling edge of SCK
- SCK can be idle in either a high or low state
- The most significant bits are shifted out first

Register Read Command in SPI Slave Mode

The Register Read command includes a command byte and address byte. The command sequence begins when the SPI master drives $\overline{SCS}$ low and sends the Read Command byte (encoded as 0x03) on the MOSI pin. Following the command byte, the master sends the address byte, which is the index to the register to be read. After receiving the least significant bit (LSB) of the address byte, the SPI slave sensor sends the contents of the selected register on the MISO pin. Finally, the master drives $\overline{SCS}$ high after it has sampled the LSB of the data byte. When reading the A/D converter, the Master may keep $\overline{SCS}$ low to read consecutive pixels up to the end of the current row. A new Register Read command must be issued to read the next row. The SPI Master must drive $\overline{SCS}$ high before beginning another command.

Register Write Command for SPI Slave Mode

The Register Write command includes a command byte and address byte followed by the data to be written. The command sequence begins when the SPI Master drives $\overline{SCS}$ low and sends the Write Command byte (encoded as 0x02) on the MOSI pin. Then the master sends the address byte, which is the index to the register to be written. Finally, the master sends the data byte and thereafter drives $\overline{SCS}$ high.

Interrupts in SPI Slave Mode

Host reads interrupt register to check for pending interrupts. Host enables interrupt. The sensor drives INTR_ low when an interrupt occurs. The host clocks out a read command.

FIFO

The 2K-bytes asynchronous FIFO. It serves as the buffer of sensor's data, which can efficiently prevent the data from loss in the mission critical application to the host CPU. Full/Empty flag is flagged whenever the condition is matched. It can also interrupt host CPU through the $\overline{INTR}$ if either flag is set.

The FIFO is initialized when one of the GETSUB, GETROW of GETIMG bit in the CTRLA register is set. The ADC output directly fill the FIFO buffer when the first row capture is completed. Then every 4 clock cycles, the FIFO receives the ADC result for the rest of the pixels converted from the row. The row capture is re-initiated once the ADC has converted the results for all of the pixels from the previous row. FIFO continuously receives the data from each ADC result every 4 clock cycles after each row capture. This process continues until FIFO buffer is Full.

The Full flag from FIFO halts the ADC to idle state. Read the CTRLA register, releases the FIFO Full flag. Also FIFO Empty flag can be set, if too frequent reading from the CTRLA register. Over reading the CTRLA register can result in the FIFO under run error. Recover from such fault condition should be performed to prevent mis-placement of the pixel data.

Function Register Descriptions

The function registers are accessed by indexed addressing. Write the index register to select a function register. Read or write the data register to access the contents of the function register. All registers can be read and written except as noted in the following descriptions.

Function Register Map

Index	Name	Description	Read/Write Access
0x01	RAL	Row Address, Low	R/W
0x02	CAL	Column Address, Low	R/W
0x04	REL	Row Address End, Low	R/W
0x05	CEL	Column Address End, Low	R/W
0x06	DTR	Discharge Time Register	R/W
0x07	DCR	Discharge Current Register	R/W
0x08	CTRLA	Control Register A	R/W
0x09	CTRLB	Control Register B	R/W
0x0A	CTRLC	Control Register C	R/W
0x0B	SRA	Status Register A	R
0x0C	PGC	Programmable Gain Control Register	R/W
0x0D	ICR	Interrupt Control Register	R/W
0x0E	ISR	Interrupt Status Register	R/W
0x0F	THR	Virtual Touch Control Register	R/W
0x10	CIDH	Chip Identification, High	R
0x11	CIDL	Chip Identification, Low	R
0x13	FCR	Control Register of FIFO	

Note: In the following descriptions, sub-image means a rectangular region of the sensor array, up to and including the entire array.

RAL 0x01

Row Address Register Low.
Reset State: 0x00

This register holds the address of the first row of a sub-image. Write 1 to bits [7:3] is inhibited.

Bit Number	Bit Name	Function
[2:0]	RA[2:0]	Low eight bits of Row Address Register

CAL 0x02

Column Address Register.
Reset State: 0x00

This register holds the address of the first column of a sub-image.

Bit Number	Bit Name	Function
[7:0]	CA[7:0]	Column Address Register

REL 0x04

Row Address End Register Low.
Reset State: 0x00

This register holds the address of the last row of a sub-image. Write 1 to bits [7:3] is inhibited.

Bit Number	Bit Name	Function
[2:0]	REND[2:0]	Low eight bits of Row Address Register

CEL 0x05

Column Address End Register.
Reset State: 0x00

This register holds the address of the last column of a sub-image.

Bit Number	Bit Name	Function
[7:0]	CEND[7:0]	Column Address Register

DTR 0x06

Discharge Time Register
Reset State: 0x00

Bit Number	Bit Name	Function
[7]	-	Reserved. Write 0 to these bits.
[6:0]	DT[6:0]	Sets the discharge time in oscillator clock periods.

DCR 0x07

Discharge Current Register
Reset State: 0x00

Bit Number	Bit Name	Function
[7:5]	-	Reserved. Write 0 to these bits.
[4:0]	DC[4:0]	Sets the discharge current rate.

There are two ways for discharge current adjustment, which include the narrow scale, when DC[4]=0 and the wide scale, when DC[4]=1. Sixteen various current settings defined by bits DC[3=0] are available for either narrow or wide scale. The difference, for the discharge current in between two consecutive settings for the wide scale, is twice as much as the narrow scale.

DC[3:0]	DC[4]=0 Discharge Current	DC[4]=1 Discharge Current
0000	0	0
0001	1/32	1/16
0010	2/32	2/16
0011	3/32	3/16
0100	4/32	4/16
0101	5/32	5/16
0110	6/32	6/16
0111	7/32	7/16
1000	8/32	8/16
1001	9/32	9/16
1010	10/32	10/16
1011	11/32	11/16
1100	12/32	12/16
1101	13/32	13/16
1110	14/32	14/16
1111	15/32	15/16*

* Note: Each setting in the table above represents the factional value to the value of 1, the 15/16 is the maximum value of discharge current that the device can be set.

CTRLA 0x08

Control Register A.
Reset State: 0x00

Write this register to initiate image conversion. Read this register to read the A/D converter.

Bit Number	Bit Name	Function
7	-	Reserved. Write 0 to this bit.
6	-	Reserved. Write 0 to this bit.
[5:4]	MVRATE [1:0]	0 = internal Multi-vibrational 12MHz ±20% 1 = internal Multi-vibrational 18MHz ±20% 2 = internal Multi-vibrational 24MHz ±20% 3 = Reserved
3	AINSEL	0=Select Array for Conversion 1=Select External Analog Input Pin and Start Conversion
2	GETSUB	Initiates Auto-increment for sub-image
1	GETIMG	Initiates Auto-increment for whole image
0	GETROW	Initiates Auto-increment for selected row

The GETSUB, GETIMG, and GETROW bits select an image access mode and initiate an A/D conversion sequence. The AINSEL bit selects the input source to the A/D converter.

Set the GETSUB bit to initiate the capture of a rectangular sub-image defined by the RAL, CAL, REL, and CEL registers. In CPU or SPI mode, the sub-image can be an arbitrary rectangle ranging from a single pixel to the entire array.

Set the GETIMG bit to initiate the capture of a whole image starting from row zero and column zero through row 7 and column 255, regardless of the RAL, CAL, REL, and CEL registers.

Set the GETROW bit to initiate the capture of a row specified by the RAL register.

Writing a 1 to any of GETSUB, GETIMG, or GETROW abandons the current image access operation and restarts at the beginning of the sub-image, image, or row. Set at most one of these three bits. If more than one these three bits are set, image conversion will not start.

Setting the GETROW bit causes the following events to happen:

- Row address loaded with contents of RAL register.
- Column address resets to zero
- Row capture automatically starts
- Analog to digital conversion of first pixel automatically starts

Setting the GETIMG bit causes the following events to happen:

- Row address resets to zero
- Column address resets to zero
- Row capture automatically starts
- Analog to digital conversion of first pixel automatically starts

Setting the GETSUB bit causes the following events to happen:

- Row address loaded with contents of RAL register
- Column address loaded with contents of CAL
- Row capture automatically starts
- Analog to digital conversion of first pixel automatically starts

Set the AINSEL bit along with one of the other three bits to begin the analog to digital conversion of the voltage on the AIN pin instead of the sensor array.

When FIFO is not enabled, read CTRLA for the result of the A/D conversion. The rising edge of $\overline{RD}$ causes the next A/D conversion to start. When FIFO is enabled, read CTRLA for the converted data stored in FIFO. Regardless of the $\overline{RD}$, ADC continuously converts the pixel result and saves it in FIFO after each completion of the row capture. Every 4 clock cycles, a new pixel result is generated from ADC.

Parameter Description	Max	Units
Rising Edge of $\overline{WR}$ to First Data Valid	28 + DT[6:0]	Clock Cycles
Rising Edge of $\overline{RD}$ to Next Data Valid	4 When FIFO is enabled 6 When FIFO is not enabled	Clock Cycles

Note: DT[6:0] refers to the contents of the Discharge Time Register.

CRTLB 0x09

Control Register B.

Reset State: CTRLB[7] = state of MODE, read only.

CTRLB[6] = 1, read only.

CTRLB[5] = 0.

CTRLB [4:0] = 0, Chip is disabled, oscillator is stopped.

Bit Number	Bit Name	Function
7	MODE	Reflects the state of the MODE pins. These bits are read-only. Writing to these bits has no effect. Write 0 to these bits.
6	RDY	This is a read-only bit that indicates the status of the A/D Converter. FFEN = 1: 0 = FIFO is empty. 1 = FIFO is not empty. FFEN = 0: 0 = ADC output is not ready. 1 = ADC output is ready. Writing this bit has no effect. Write 0 to this bit.
5	WAITEN	Set this bit to enable the wait state function for WAIT_pin control 0 = wait state mode is not enabled. 1 = wait state mode is enabled.
4	-	Reserved. Write 0 to this bit.
3	VTHEN	Set this bit to enable the VirtualTouch function.
2	AUTOINCEN	0 = Column and row addresses do not automatically increment after the A/D converter is read. 1 = Column addresses increment and another A/D conversion is initiated after the A/D converter is read. The row address increments at the end of each column.
1	XTALSEL	In CPU and SPI mode this bit selects the clock source for the digital logic. 0 = Selects the internal 12 MHz multi-vibrator. 1 = Selects the XTAL1 pin.
0	ENABLE	0 = Place the sensor array, digital, and analog block into low-power state (12 MHz clock is halted, A/D Converter is shut down). 1= Enable the sensor array, digital, and analog blocks (12 MHz clock and A/D Converter are enabled).

CTRLC 0x0A

Control Register C. This register controls the behavior of general output port pins P0 and P1.
Reset State: 0x00

Bit Number	Bit Name	Function
[7:5]	PT1[2:0]	Programs the toggle rate of the P1 pin. If PT1[2:0] = 000, then the P1 pin follows the state of the P1 bit. Otherwise PT1[2:0] selects the clock divisor to generate a square wave on the P1 pin. 000 = P1 pin follows state of bit P1. 001 = clock divided by 2^{24}. 010 = clock divided by 2^{23}. 011 = clock divided by 2^{22}. 100 = clock divided by 2^{21}. 101 = Reserved. 110 = Reserved. 111 = Reserved.
[4:2]	PT0[2:0]	Programs the toggle rate of the P0 pin. If PT0[2:0] = 000, then the P0 pin follows the state of the P0 bit. Otherwise PT0[2:0] selects the clock divisor to generate a square wave on the P0 pin. 000 = P0 pin follows state of bit P0. 001 = clock divided by 2^{24}. 010 = clock divided by 2^{23}. 011 = clock divided by 2^{22}. 100 = clock divided by 2^{21}. 101 = Reserved. 110 = Reserved. 111 = Reserved.
1	P1	General Purpose Output Port. When PT1[2:0] bits are 000, this bit controls the P1 pin. 0 = P1 pin low. 1 = P1 pin high.
0	P0	General Purpose Output Port. When PT0[2:0] bits are 000, this bit controls the P0 pin. 0 = P0 pin low. 1 = P0 pin high.

SRA 0x0B

Status Register A. Read Only. This register shadows the state of CTRLA.
Reset State: 0x00

Bit Number	Bit Name	Function
7	-	Reserved. Returns 0.
6	-	Reserved. Returns 0.
[5:4]	MVRATE [1:0]	0 = internal Multi-vibration at 12MHz ± 20% 1 = internal Mulit-vibration at 18MHz ± 20% 2 = internal Multi-vibration at 24MHz ± 20% 3 = Reserved
3	AINSEL	This bit is set or cleared when the AINSEL bit (CTRLA bit 3) is set or cleared by software.
2	GETSUB	This bit is set when the GETSUB bit (CTRLA bit 2) is set by software. This bit is cleared after the last byte is read.
1	GETIMG	This bit is set when the GETIMG bit (CTRLA bit 1) is set by software. This bit is cleared after the last byte is read.
0	GETROW	This bit is set when the GETROW bit (CTRLA bit 0) is set by software. This bit is cleared after the last byte is read.

PGC 0x0C

Programmable Gain Control Register.
Reset State: 0x00

Bit Number	Bit Name	Function
[7:4]	-	Reserved. Write 0 to these bits. Returns 0 when read.
[3:0]	PG[3:0]	Sets the gain of the amplifier. 0000 = 1.0 (default) 0001 = 0.25 0010 = 0.50 0011 = 0.75 0101 = 1.25 0110 = 1.50 0111 = 1.75 1010 = 2.0 1011 = 3.0 1100 = 4.0 1101 = 5.0 1110 = 6.0 1111 = 7.0

ICR 0x0D

Interrupt Control Register.
Reset State 0x00.

This register controls the behavior of the interrupt source of the fingerprint sensor. Interrupt request 0 corresponds to the finger detect interrupt.

Set bits IEO to enable the corresponding interrupt. Disabling an interrupt prevents the interrupt event from causing the chip to assert $\overline{\text{INTR}}$. However, the interrupt event is not prevented from setting its corresponding bit in the ISR register.

Set bits IM[0] to prevent an interrupt event from setting the corresponding bit in the ISR. Setting or clearing IM[0] will not clear ISR bits IR[0].

Set bits IT[0] to program the interrupts as edge or level sensitive.

Bit Number	Bit Name	Function
7	-	This bit is reserved.
6	IP0	0=Virtual Touch Interrupt is Falling Edge or Active Low 1= Virtual Touch Interrupt is Rising Edge or Active High
5	-	This bit is reserved.
4	IT0	0=Virtual Touch Interrupt is Edge Triggered 1= Virtual Touch Interrupt is Level Triggered
3	-	This bit is reserved.
2	IM0	0=Vitual Touch Interrupt Not Masked 1= Virtual Touch Interrupt Masked
1	-	This bit is reserved.
0	IE0	0=Vitual Touch Interrupt Disabled 1=Vitual Touch Interrupt Enabled

ISR 0x0E

Interrupt Status Register.
Reset State ISR[7:0] = 0.

Read this register to determine source(s) of interrupt(s).
Write a 1 to IR[5:4, 0] to acknowledge and clear the corresponding interrupt bit.

Bit Number	Bit Name	Function
7	IS3	Reflect the state of the FIFO full status.
6	IS2	Reflect the state of the FIFO empty status.
5	IR3	FIFO full interrupt request pending if IM3=0.
4	IR2	FIFO empty interrupt request pending if IM2=0.
3	-	
2	IS0	Reflects the state of Virtual Touch status.
1	-	
0	IR0	Virtual Touch interrupt request pending if IM0=0.

THR 0x0F

Threshold voltage and sharing capacitor control register of Virtual Touch. Reset state THR[7:0] = 0x00.

Bit Number	Bit Name	Function
[7:4]	THV[3:0]	Threshold voltage level.
[3:0]	THC[3:0]	Sharing capacitor size.

CIDH 0x10

Chip Identification Register High. This register holds the high order byte of the chip identification word.

Bit Number	Bit Name	Function
[7:0]	CIDH[7:0]	Returns 0x31 when read.

CIDL 0x11

Chip Identification Register Low. This register holds the low order byte of the chip identification word.

Bit Number	Bit Name	Function
[7:0]	CIDL[7:0]	The return value depends on the Revision of the chip. Returns 0x10 for the first revision.

FCR 0x13

FIFO Control Register.

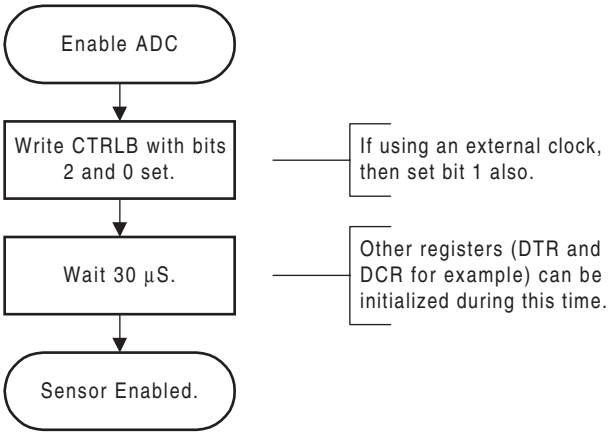
Reset State 0x00.

Write this register to determine FIFO operation and its interrupt control. FIFO is reset when writing to GETIMG, GETSUB or GETROW. FIFO underrun/overrun can occur if the empty/full flag is ignored. It is user's reseponsibility to handle such fault events.

Bit Number	Bit Name	Function
[7:5]	-	Reserved
4	IM3	0 = FIFO full Interrupt request is not masked. 1 = FIFO full Interrupt request is masked.
3	IM2	0 = FIFO empty Interrupt request is not masked. 1 = FIFO empty Interrupt request is masked.
2	IE3	0 = FIFO full Interrupt request is disabled. 1 = FIFO full Interrupt request is enabled.
1	IE2	0 = FIFO empty Interrupt request is disabled. 1 = FIFO empty Interrupt request is enabled.
0	FFEN	0 = FIFO function disabled. 1 = FIFO function enabled. The auto-increment is enabled disregards the AUTOINCEN bit of CTRLB register.

Sensor Initialization

The sensor should be enabled and its image parameters adjusted before beginning a GETIMG, GETROW, or GETSUB operation.



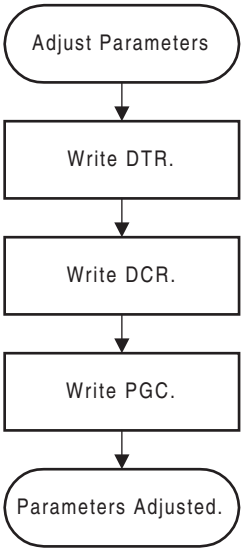
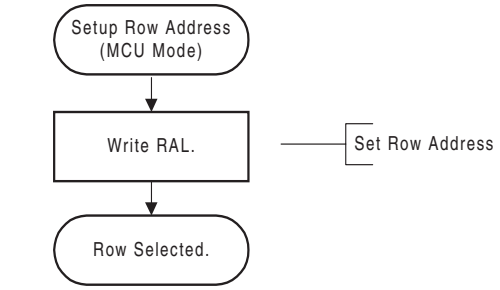


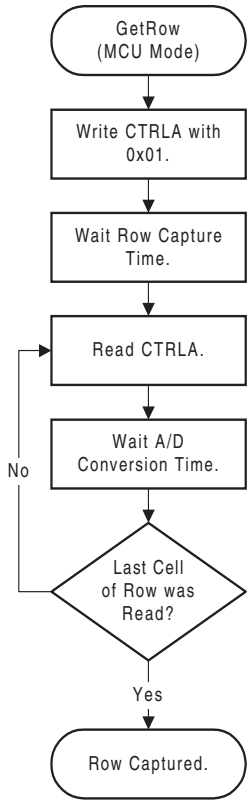
Image Retrieval

Microprocessor Interface

Get Row with FIFO Disabled

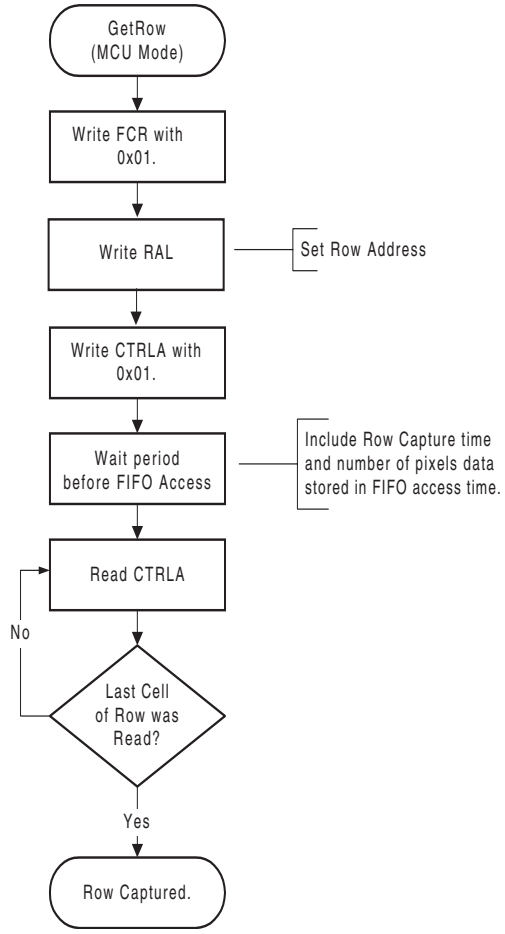
First load the RAL register with the address of the row to be fetched. Then write the CTRLA register to initiate a GETROW operation. Finally, read the CTRLA register 256 times to retrieve the row data.





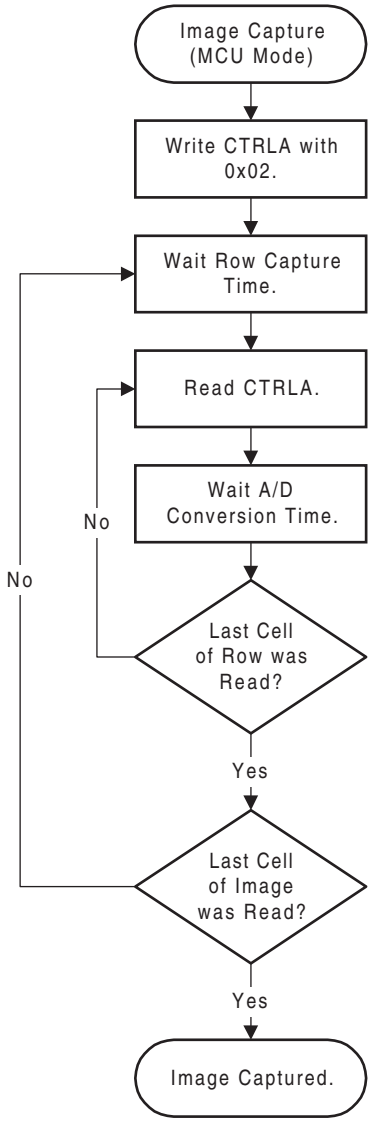
Get Row with FIFO Enabled

First load the RAL register with the address of the row to be fetched. Then write the CTRLA register to initiate a GETROW operation. Finally, read the CTRLA register 256 times to retrieve the row data. The wait period before reading the CTRLA can vary depending on the MPU read access frequency. Properly adjusted the read frequency so that the FIFO empty state can be avoided.



Get Whole Image with FIFO disabled

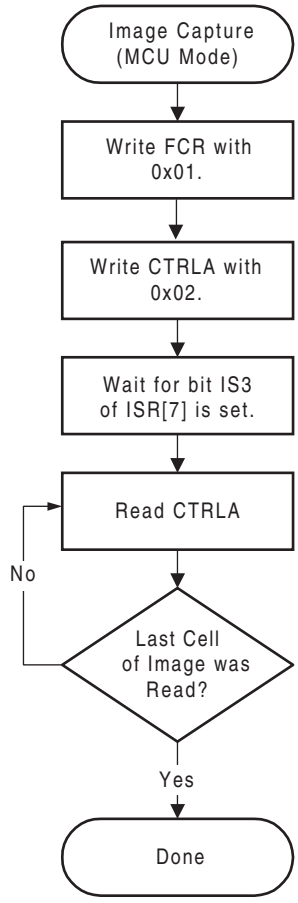
No row or column registers need to be loaded prior to starting a GETIMG operation. The sensor will automatically begin A/D conversion at row zero, column zero.



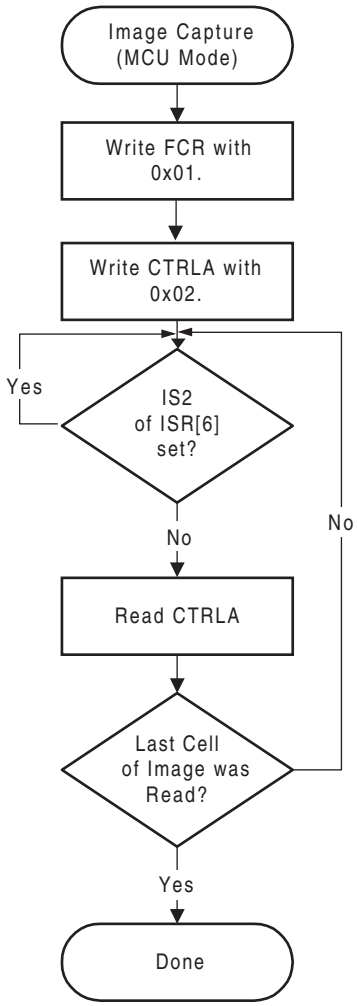
Get Whole Image with FIFO enabled

No row or column registers need to be loaded prior to starting a GETIMG operation. The sensor will automatically begin A/D conversion at row zero, column zero.

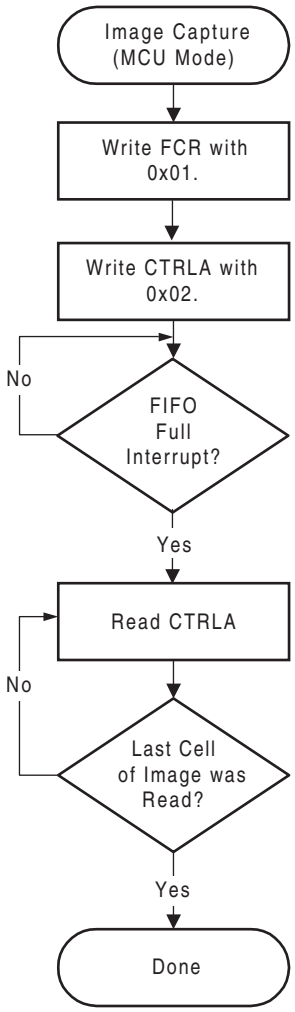
(i) with FIFO full flag pulling



(ii) with FIFO empty flag pulling

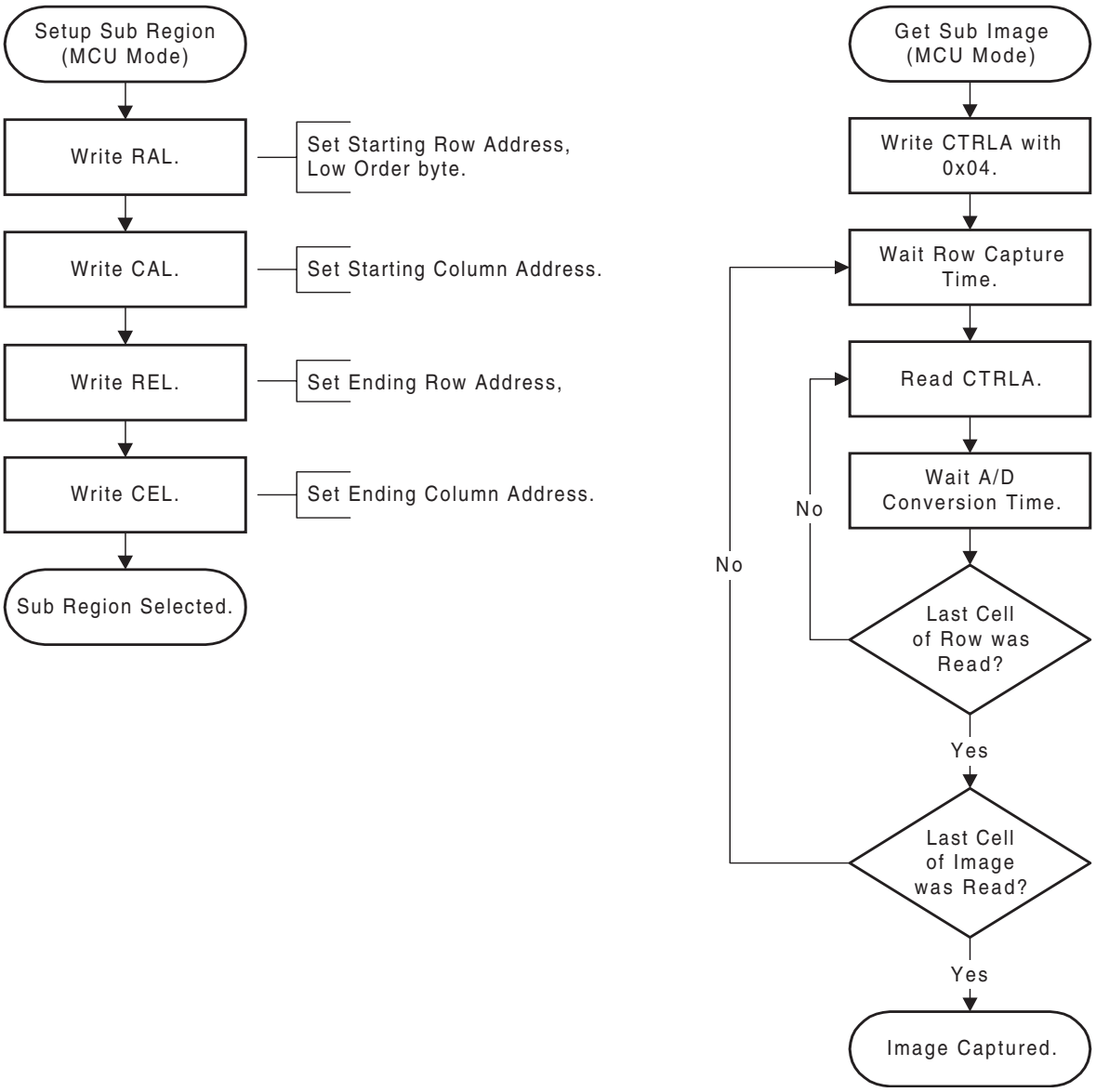


(iii) with FIFO interrupt enabled



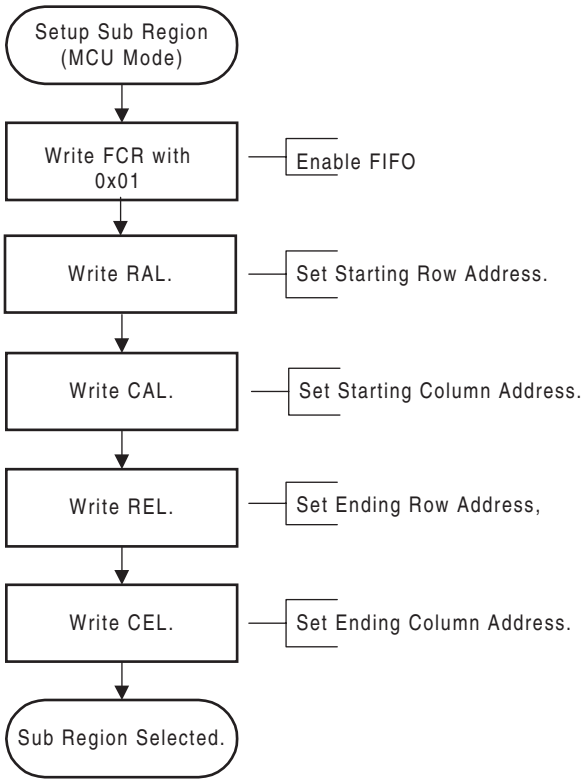
Get Sub-Image with FIFO disabled

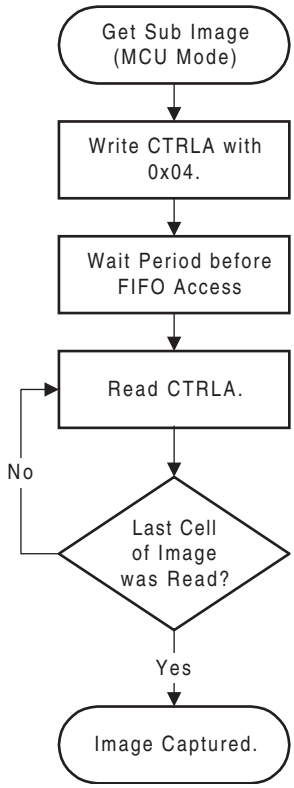
First, load the RAL, and CAL registers with the starting row and column address of the sensor sub-region. Then load registers REL, and CEL with the ending row and column address of the sensor sub-region. Write the CTRLA register to initiate a GETSUB operation. Finally, read CTRLA register until the sub-image has been retrieved. The RAL, CAL, REL, and CEL registers do not have to beloaded before each GETSUB operation unless a different sensor sub-region is to be captured.



Get Sub-Image with FIFO enabled

First, load the RAL and CAL with the starting row and column address of the sensor sub-region. Then, load registers REL and CEL with the ending row and column address of the sensor sub-region. Write the CTRLA register to initiate a GETSUB operation. Finally, read CTRLA register until the sub-image hass been retrieved. The RAL, CAL, REL and CEL registers do not have to be loaded before each GETSUB operation unless a different sensor sub-region is to be captured. The wait period before reading the CTRLA can vary depending on the MPUs read access frequency. Properly adjust the read frequency so that the FIFO empty state can be avoided. Retrieving the sub-image data can also be done by either the FIFO full/empty flag pulling, or the FIFO full imterrupting.

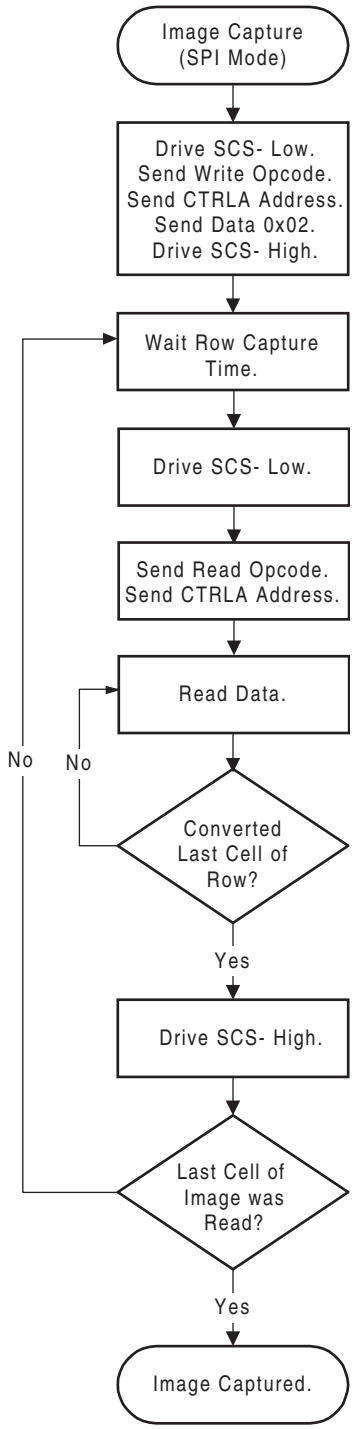




Serial Peripheral Interface with FIFO disabled

The "Get Image," "Get Sub-Image," and "Get Row" operations are initiated by writing the same registers as described in the microprocessor interface, except that the commands are written to the MOSI pin and the data is read back on the MISO pin. However, in SPI mode, an image or sub-image cannot be retrieved by issuing a single Register Read Command and shifting in the entire image; a separate Register Read Command must be issued prior to reading each row.

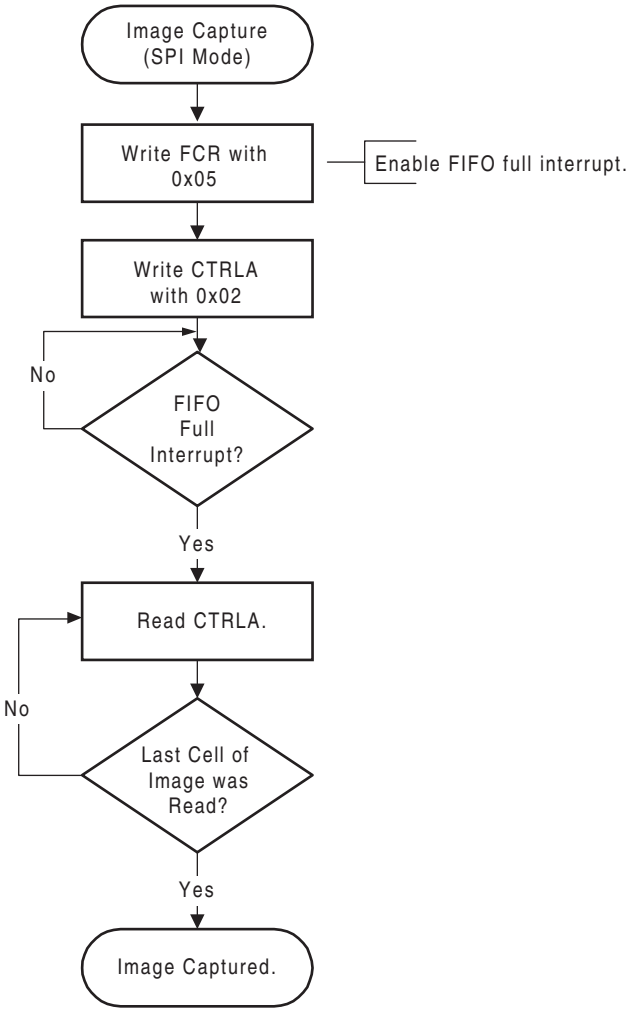
Get Image



Serial Peripheral Interface with FIFO enabled

Unlike the SPI mode with FIFO disabled, an image or sub-image can be retrieved by issuing a single RegisterRead Command and shifting in the entire image. No separate Register Read Command is needed prior to reading each row. Enable FIFO fill interrupt and wait for interrupt form FIFO before accessing the image data.

Retrieving the image data can also be done by pulling the FIFO full/empty flags.



Absolute Maximum Ratings

Symbol	Rating	Value	Unit
V_{DD}	Power Supply Voltage	+5.0	V
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to VSS	-0.5 to +5.0	V
I_{OUT}	Output Current per I/O	12.0	mA
T_{STG}	Storage Temperature	-65 to +150	°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability.

Operating Range

Symbol	Description	Min	Max	Unit
V_{DD}	Supply Voltage	2.7	3.3	V
T_A	Ambient Temperature	-20	+85	°C

DC Characteristics

(VDD=2.7V)

Symbol	Description	Test Conditions	Min	Max	Units
V_{IL}	Input LOW Voltage	VDD = 2.5V	-0.5	0.5	V
V_{IH}	Input HIGH Voltage	–	2.0	VDD	V
V_{OL}	Output LOW Voltage	VDD = MIN, IOL = 6 mA	-	0.4	V
V_{OH}	Output HIGH Voltage	VDD = MIN, IOH = -6 mA	2.0	-	V
I_{LI}	Input Leakage Current	VDD = MAX, VIN = VSS to VDD	-5.0	5.0	µA
I_{LO}	Output Leakage Current	VDD = MAX, VOUT = VSS to VDD, CE0- = VIH or CE1 = VIL	-5.0	5.0	µA

(VDD=3.3V)

Symbol	Description	Test Conditions	Min	Max	Units
V_{IL}	Input LOW Voltage	VDD = 3.0V	-0.5	0.6	V
V_{IH}	Input HIGH Voltage		2.0	VDD	V
V_{OL}	Output LOW Voltage	VDD = 3.6V, IOL = 8 mA	-	0.4	V
V_{OH}	Output HIGH Voltage	VDD = 3.0V, IOH = -8 mA	2.4	-	V
I_{LI}	Input Leakage Current	VDD = 3.6V VIN = VSS to VDD	-5.0	5.0	µA
I_{LO}	Output Leakage Current	VDD = 3.6V, VOUT = VSS to VDD, CE0- = VIH or CE1 = VIL	-5.0	5.0	µA

Power Supply Consumption

Symbol	Description	Test Conditions	Max	Units
(Microprocessor Mode, VDD=2.7V f_{OSC} = 12MHz)				
I_{DD}	Digital Current, Dynamic		4	mA
I_{DDSB}	Digital Current, Standby		1	mA
I_{DDPDF}	Digital Current, Power Down with Auto Finger Detection Enabled		10	µA
I_{DDPD}	Digital Current, Power Down		10	µA
I_{DDA}	Analog Current, Dynamic		8	mA
I_{DDASB}	Analog Current, Standby		5	mA
I_{DDAPDF}	Analog Current, Power Down with Auto Finger Detection Enabled		200	µA
I_{DDAPD}	Analog Current, Power Down		10	µA
(SPI Slave Mode, VDD=2.7V, f_{OSC} = 12MHz, SCLK = 12MHz)				
I_{DD}	Digital Current, Dynamic		4	mA
IDDSB	Digital Current, Standby		1	mA
I_{DDPDF}	Digital Current, Power Down with Auto Finger Detection Enabled		10	µA
I_{DDPD}	Digital Current, Power Down		10	µA
I_{DDA}	Analog Current, Dynamic		8	mA
I_{DDASB}	Analog Current, Standby		5	mA
I_{DDAPDF}	Analog Current, Power Down with Auto Finger Detection Enabled		200	µA
I_{DDAPD}	Analog Current, Power Down		10	µA
(Microprocessor Mode, VDD=3.3V, f_{OSC} = 12MHz)				
I_{DD}	Digital Current, Dynamic		5	mA
I_{DDSB}	Digital Current, Standby		1	mA
I_{DDPDF}	Digital Current, Power Down with Auto Finger Detection Enabled		10	µA
I_{DDPD}	Digital Current, Power Down		10	µA
I_{DDA}	Analog Current, Dynamic		10	mA
I_{DDASB}	Analog Current, Standby		6	mA
I_{DDAPDF}	Analog Current, Power Down with Auto Finger Detection Enabled		200	µA
I_{DDAPD}	Analog Current, Power Down		10	µA
(SPI Slave Mode, VDD=3.3V, f_{OSC} = 12MHz, SCLK = 12MHz))				
I_{DD}	Digital Current, Dynamic		5	mA
I_{DDSB}	Digital Current, Standby		1	mA
I_{DDPDF}	Digital Current, Power Down with Auto Finger Detection Enabled		10	µA
I_{DDPD}	Digital Current, Power Down		10	µA
I_{DDA}	Analog Current, Dynamic		10	mA
I_{DDASB}	Analog Current, Standby		6	mA
I_{DDAPDF}	Analog Current, Power Down with Auto Finger Detection Enabled		200	µA
I_{DDAPD}	Analog Current, Power Down		10	µA

AC Characteristics

Microprocessor Bus Mode

Read Cycle

Symbol	Description	Min	Max	Units
t_{ACC}	Address to Output Delay	-	35	ns
t_{CE}	Chip Select to Output Delay	-	35	ns
t_{OE}	Read Enable to Output Delay	-	35	ns
t_{OH}	Output Hold Time from Address, $\overline{CS0}$, CS1, or $\overline{RD}$, which ever occurs first	0	-	ns
t_{DF}	$\overline{RD}$ high to Output High Z	-	5	ns
t_{DF}	$\overline{CS0}$ high or CS1 low to Output High Z	-	5	ns
t_{WT}	Read Enable to $\overline{WAIT}$ low	-	20	ns
t_{RIN}	Read Enable to $\overline{INTR}$ low due to FIFO empty	-	30	ns

Write Cycle

Symbol	Description	Min	Max	Units
t_{AS}	Address Setup to $\overline{WR}$ low	0	-	ns
t_{CS}	$\overline{CS0}$ Setup to $\overline{WR}$ low	0	-	ns
t_{CS}	CS1 Setup to $\overline{WR}$ low	0	-	ns
t_{AH}	Address Hold Time from $\overline{WR}$ high	5	-	ns
t_{CH}	$\overline{CS0}$ Hold Time from $\overline{WR}$ high	0	-	ns
t_{CH}	CS1 Hold Time from $\overline{WR}$ high	0	-	ns
t_{WP}	$\overline{WR}$ Pulse Width Low	10	-	ns
t_{WPH}	$\overline{WR}$ Pulse Width High	10	-	ns
t_{DS}	Data Setup Time to $\overline{WR}$ low	8	-	ns
t_{DH}	Data Hold Time to $\overline{WR}$ high	5	-	ns
t_{INT}	$\overline{WR}$ end to INTR- high. For interrupt acknowledge with 4.7KΩ pull-up	500	-	ns

SPI Slave Mode

Symbol	Description	Min	Max	Units
f_{SCK}	SCLK Clock Frequency	-	20	MHz
t_{CSS}	$\overline{SCS}$ Setup Time	40	-	ns
t_{CSH}	$\overline{SCS}$ Hold Time	40	-	ns
t_{WL}	SCLK Low	40	-	ns
t_{WH}	SCLK High	40	-	ns
t_{CS}	$\overline{SCS}$ High Time	40	-	ns
t_{SU}	Data-In Setup Time	20	-	ns
t_{H}	Data-In Hold Time	20	-	ns
t_{V}	Data-Out Valid Time	20	30	ns
t_{HD}	Data-Out Hold Time	0	-	ns
t_{DIS}	Data-Out Disable Time	-	100	ns

Timing Diagrams

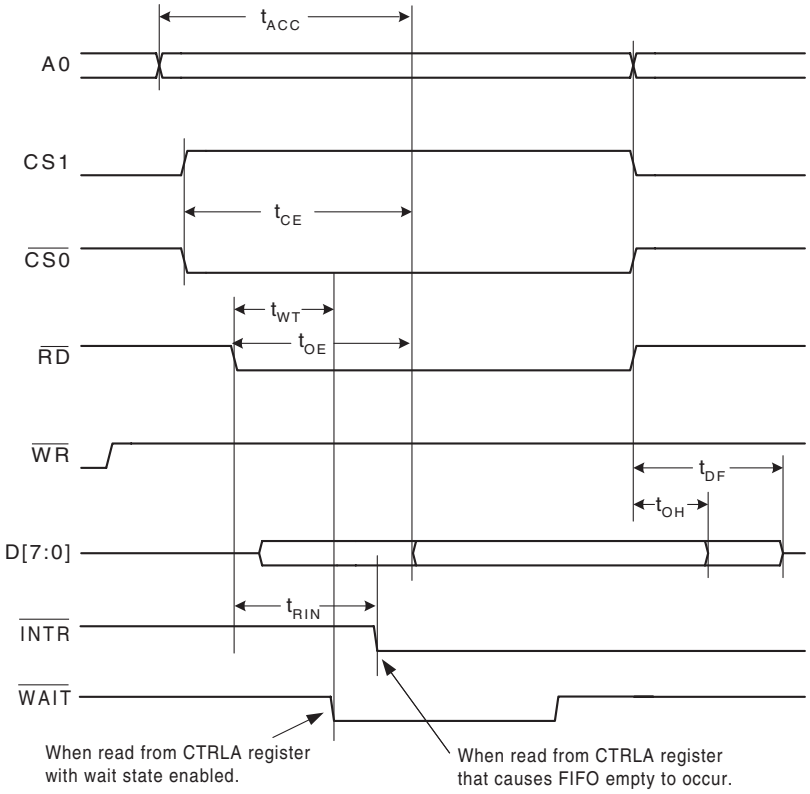


Figure 1. Microprocessor Mode Read Cycle

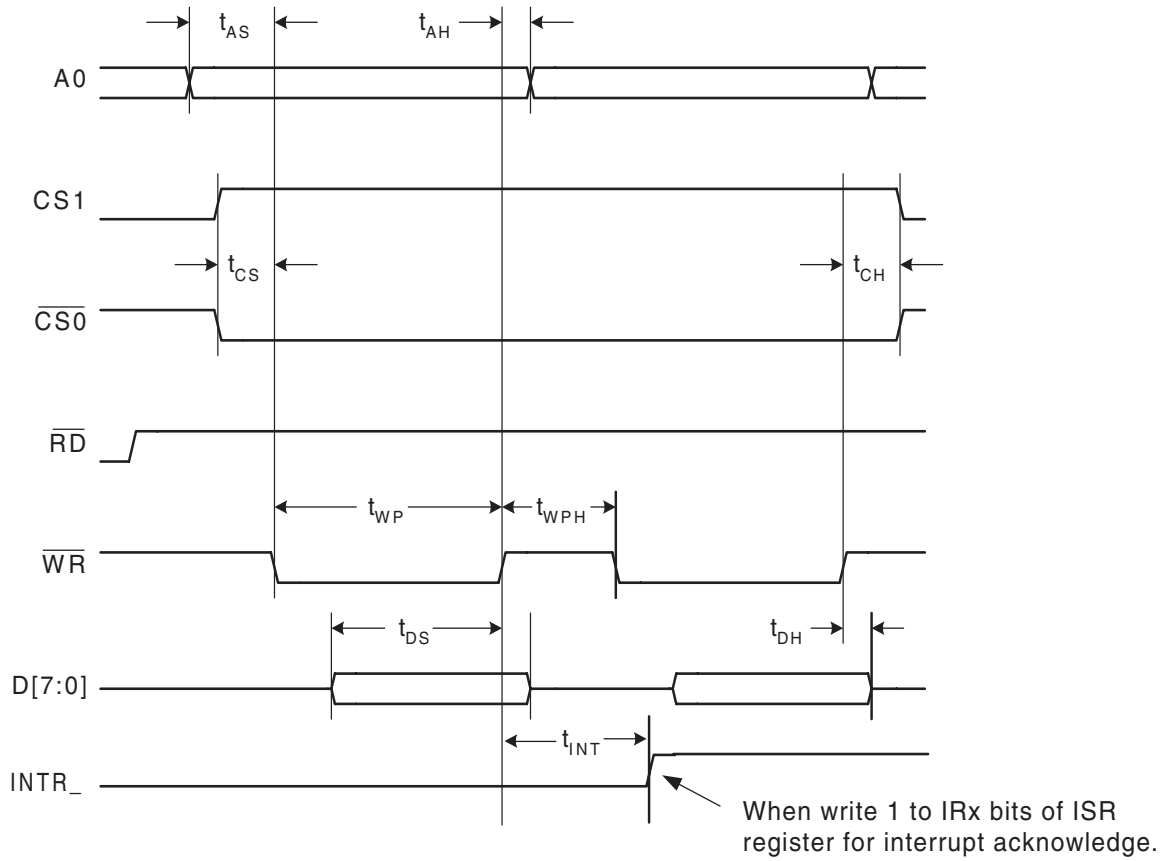


Figure 2. Microprocessor Mode Write Cycle

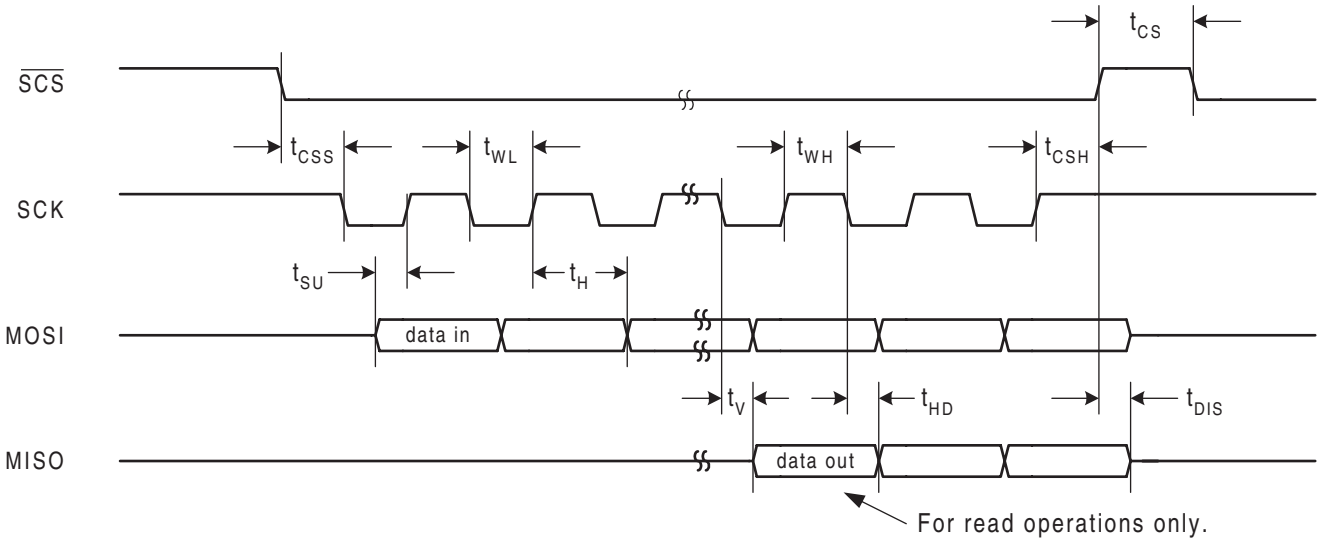


Figure 3. SPI Slave Mode Timing

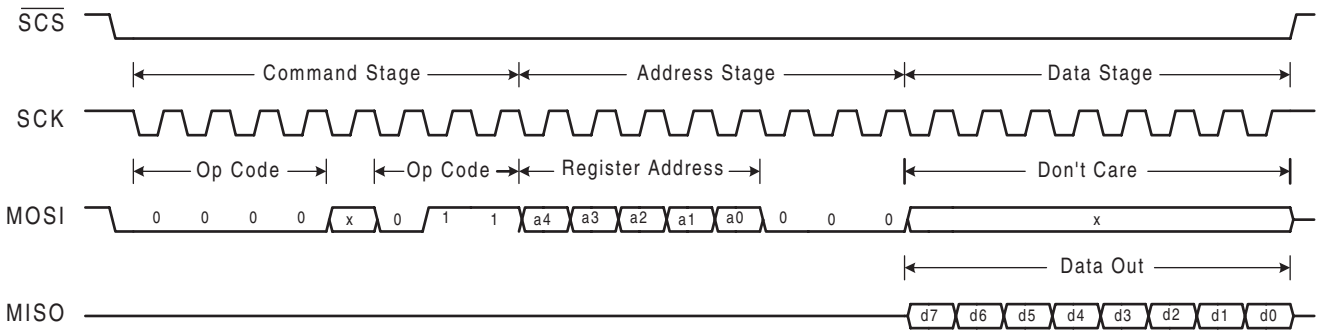


Figure 4: SPI Slave Mode Read Operation

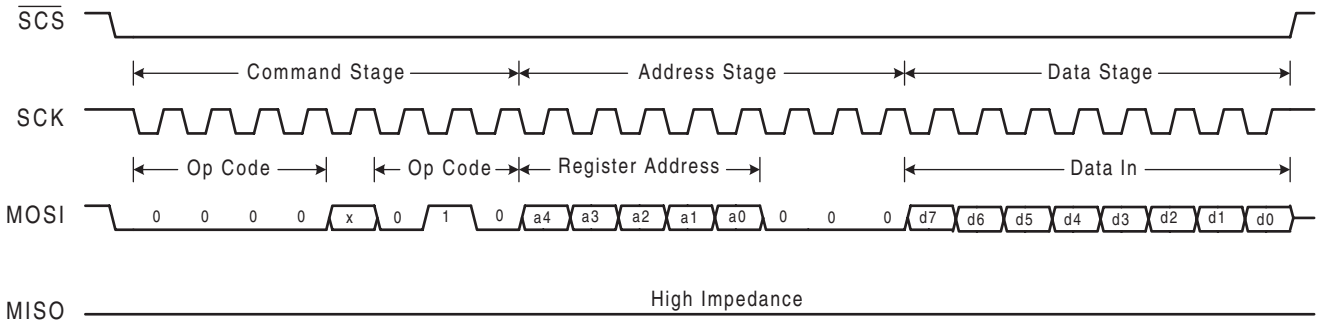
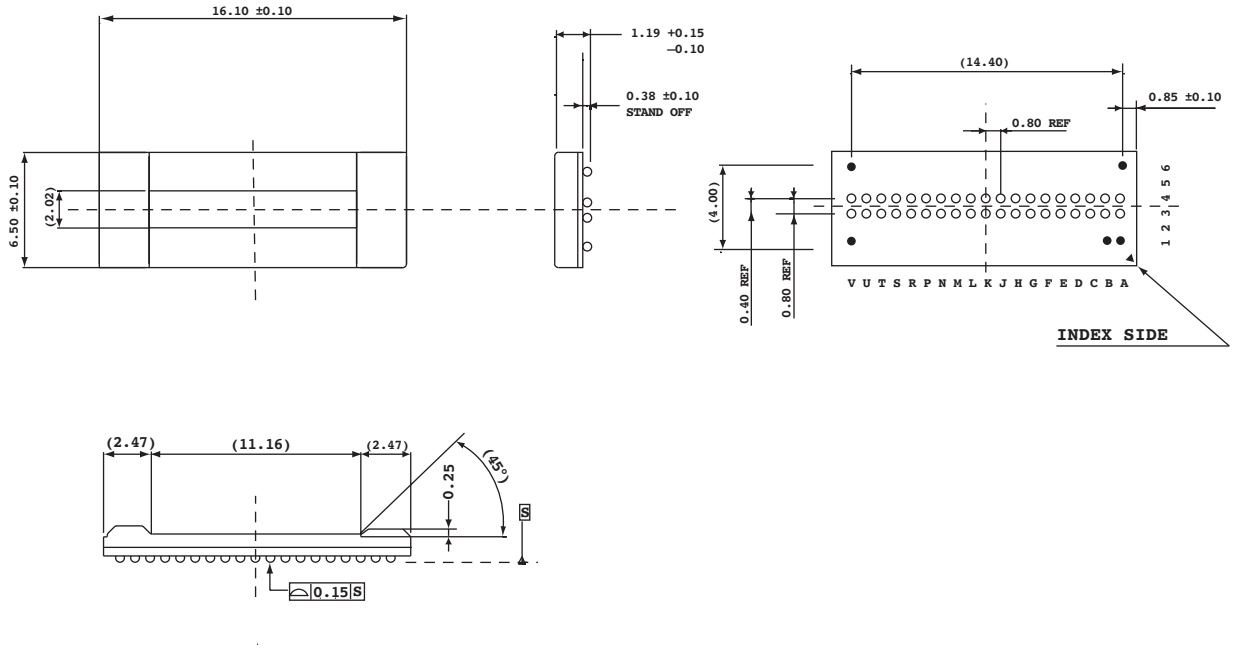


Figure 5: SPI Slave Mode Write Operation

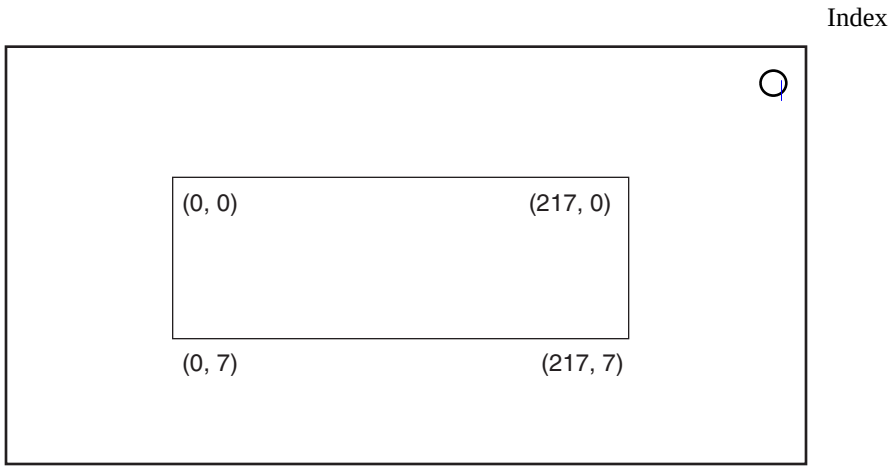
Solid State Fingerprint Sweep Sensor™

Physical Dimensions

(all units in mm)



Array Orientation



Appendix A

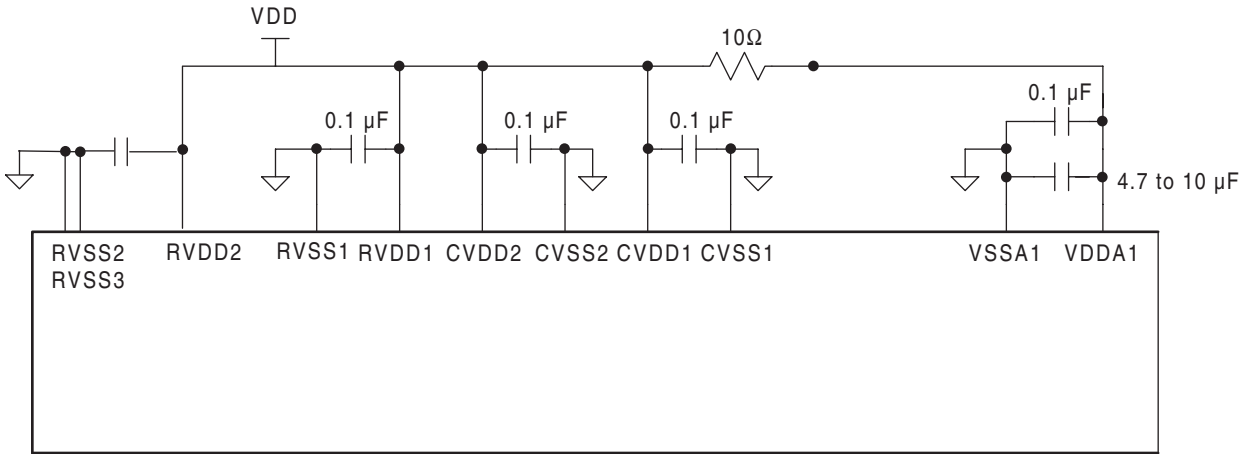
Recommended Power and Ground Connections

The following describes the recommended method for reducing image noise to get the best image from the sensor.

VDDA1 is the analog power supply pin. VSSA1 is the ground return. Connect one bulk capacitor (4.7µF to 10µF) and two 0.1µF capacitors in parallel between analog power and ground to provide filtering of low and high frequency noise. Place the bulk capacitor near VDDA1. Separate VDDA1 from the digital power pins through a 10 ohm resistor.

CVDD1, CVDD2, RVDD1 and RVDD2 are the digital power supply pins. CVSS1, CVSS2, RVSS, RVSS2 and RVSS3 are the ground returns. Place 0.1µF capacitors between digital power and ground, as close to the pins as possible.

Input signals that are to be tied high should not be shorted directly to VDD, but connected through a 1K to 10K ohm resistor in order to maximize ESD immunity of the sensor. A single resistor may be used for all inputs that are tied high.



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